

Fixed and Variable Frequency Digital Control Architectures in Switched Mode Power Converters and FPGA-based Prototyping

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Outline

- Embedded Power Management (EPM) Lab, EE Department, IIT Kharagpur
- Digital Control in Power Electronics Converters – Growing industry trends
- Level of digitization in digitally controlled switched-mode power converters
- Fixed/variable-frequency digital control – design and tuning with case studies
- Developed ONLINE courses – useful for skilled manpower development
- Summarizing Digital Control course outlines, pedagogical resources, and usefulness

Indian Institute of Technology (IIT) Kharagpur



First IIT (est. in 1951), largest & most diversified IIT

Department of **Electrical Engineering** started in 1951



- ❑ **Embedded Power Management**
(EPM) lab started in 2014
- ❑ **Research: Digital control, WBG-**
based **high power density SMPC**



Pedagogy and Industry Training Programs

- **Delivered industry training/tutorial on Modeling and Control of Switched Mode Power**

Converters for ST Microelectronics, Qualcomm, NXP, Texas Instruments, HCL Technology

- **Developed NPTEL Online Certification Course on “Control and Tuning Methods in Switched**

Mode Power Converters” – [Available on YouTube](#)

- **Introduced NPTEL Online Certification Course on “Digital Control in Switched Mode**

Power Converters and FPGA-based Prototyping” – [Available on YouTube](#)

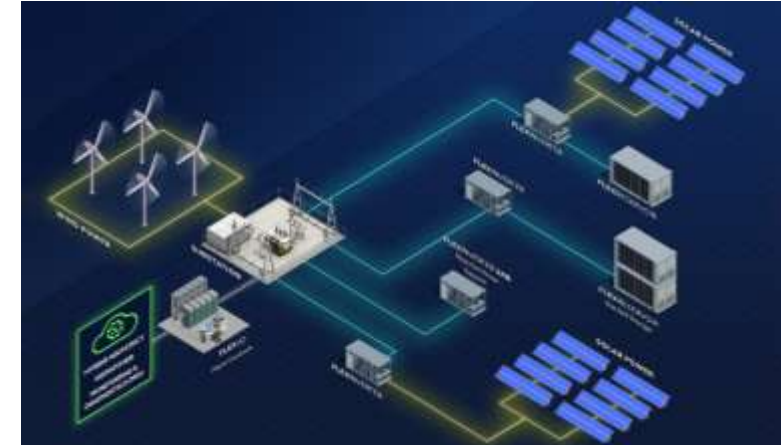
Digital Control in Emerging Power Electronics Applications



Automotive electronics [[Qualcomm](#)]



Data center [[ABB](#)]



Renewable, microgrid [[GE](#)]



Consumer Electronics [[EDN](#)]



5G Communication [[EE Times](#)]

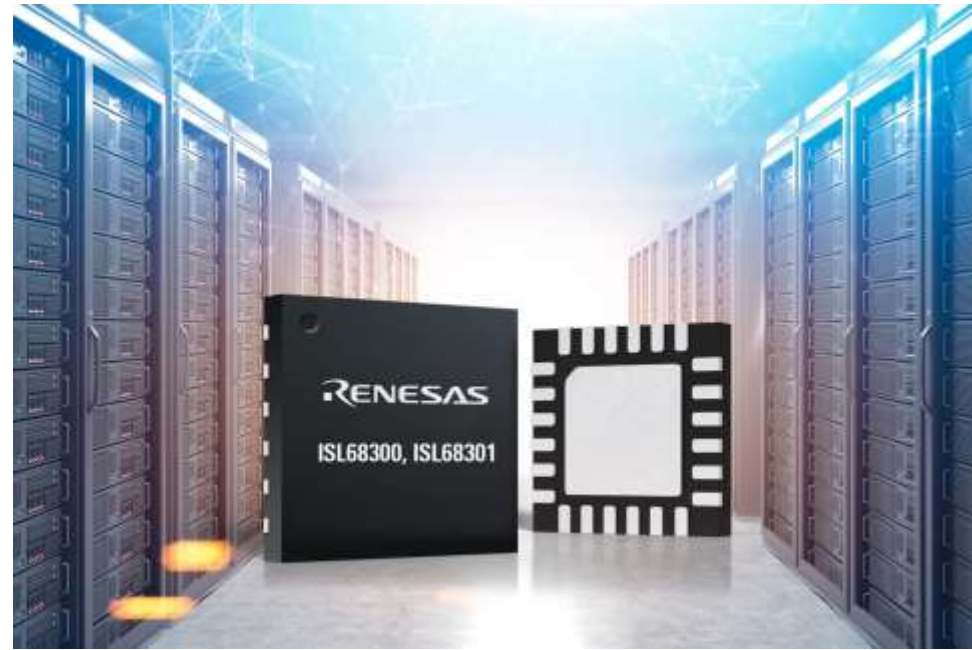


DC fast chargers [[Delta](#)]

Digital Power Control ICs



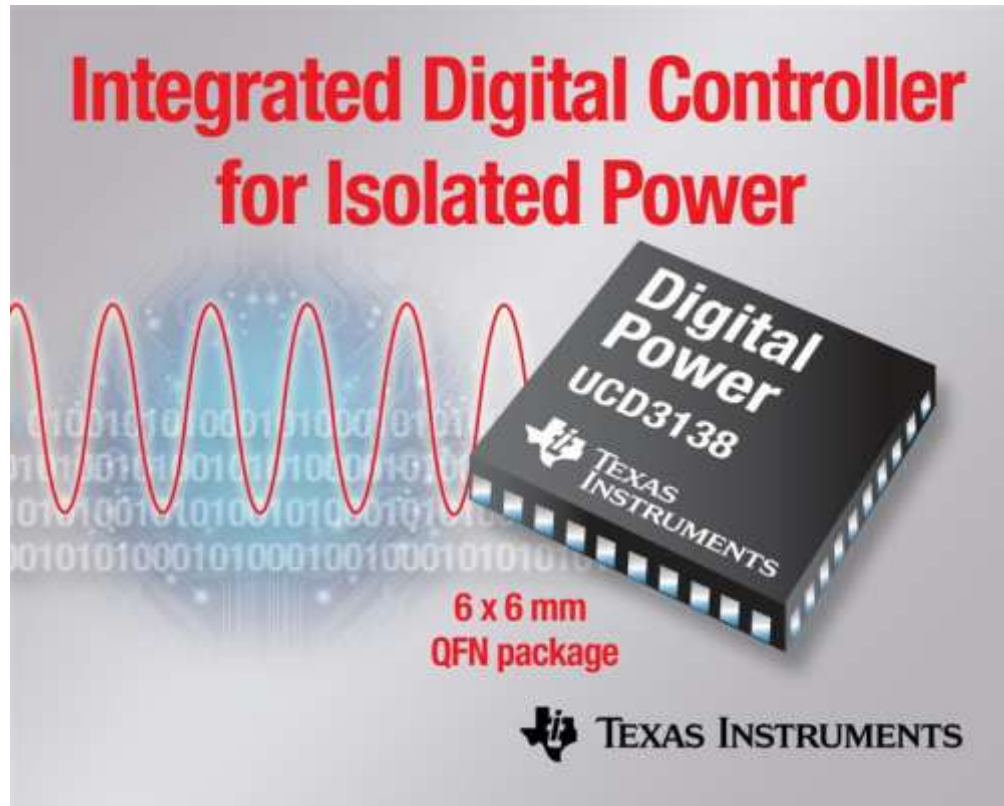
Renesas digital power for data center



Renesas digital power for cloud server

- ❑ *ChargeMode Control for Fast Transient Performance*
- ❑ *Inherently stable current loop without external ramp compensation*

Digital Power Control ICs



TI digital power solution

- Smart features for high peak/light load efficiency, soft on-off control, etc.
- Single digital controlled IC supports various isolated converter topologies
- Control of multiple isolated converters using a single controller IC
- All protection circuits included

Digital Power Control IC for PFC-LLC



- Integrated start-up logic with low standby power
- Digital multi-mode PFC-LLC combo solution
- Multi-mode PFC for optimized efficiency curve
- Reduced component count – smaller size
- Parameter configurations

Infineon digital power

SiC-based 3.6 kW Digitally Controlled Totem Pole PFC

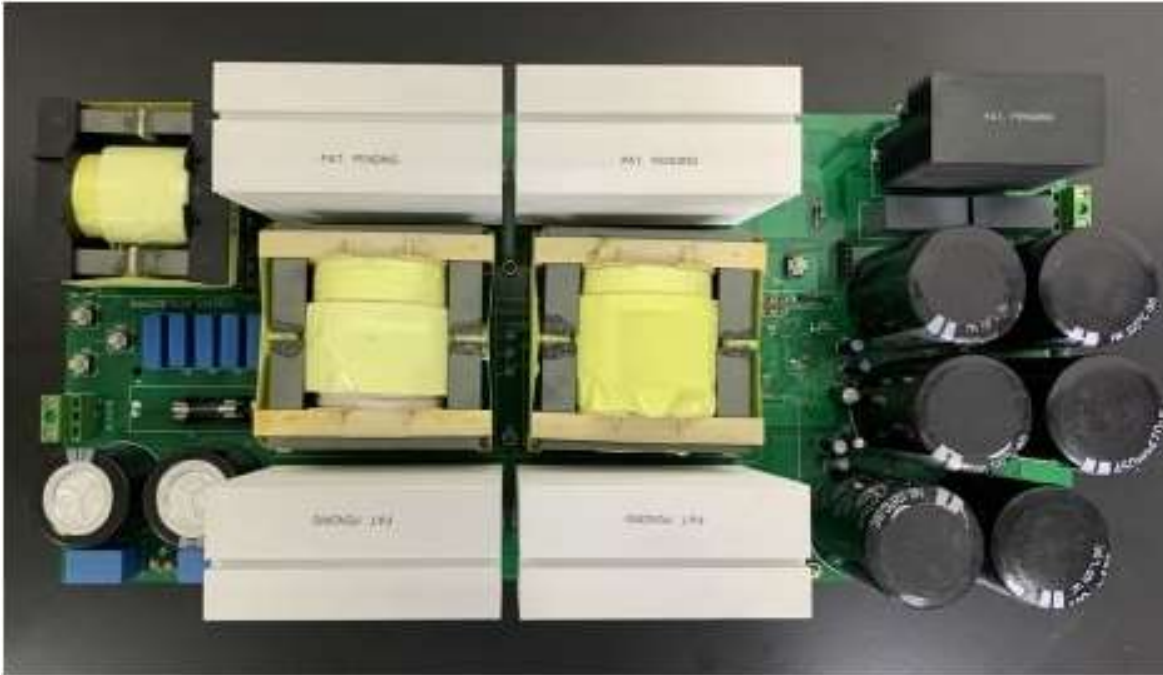


*STMicroelectronics digitally controlled
3.6kW Totem Pole PFC converter
using STM32 microcontroller*

Source: [STEVAL-DPSTPFC1](#)

- Input AC voltage: 85 to 264 V (RMS)
- Input line frequency: 45 to 65 Hz
- Output DC Voltage: 400 – 450 V
- Fully digital control solution
- Peak efficiency 97.5% with THD 3.7%
- STM32F334 uC firmware support

Digitally Controlled 6 kW LLC Resonant Converter for EV Charger



STMicroelectronics digitally controlled 6kW LLC converter using STM32 microcontroller

Source: [STDES-6KWHVDCDC](#)

- Input Voltage: 700V to 800V
- Output voltage/power: 200 – 1000 V
- Fully digital control solution
- Peak efficiency 98%
- STM32G474 uC firmware support
- Design presented in Lectures ~84, 85

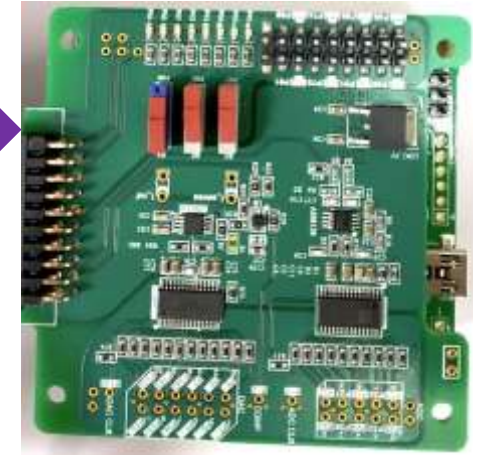
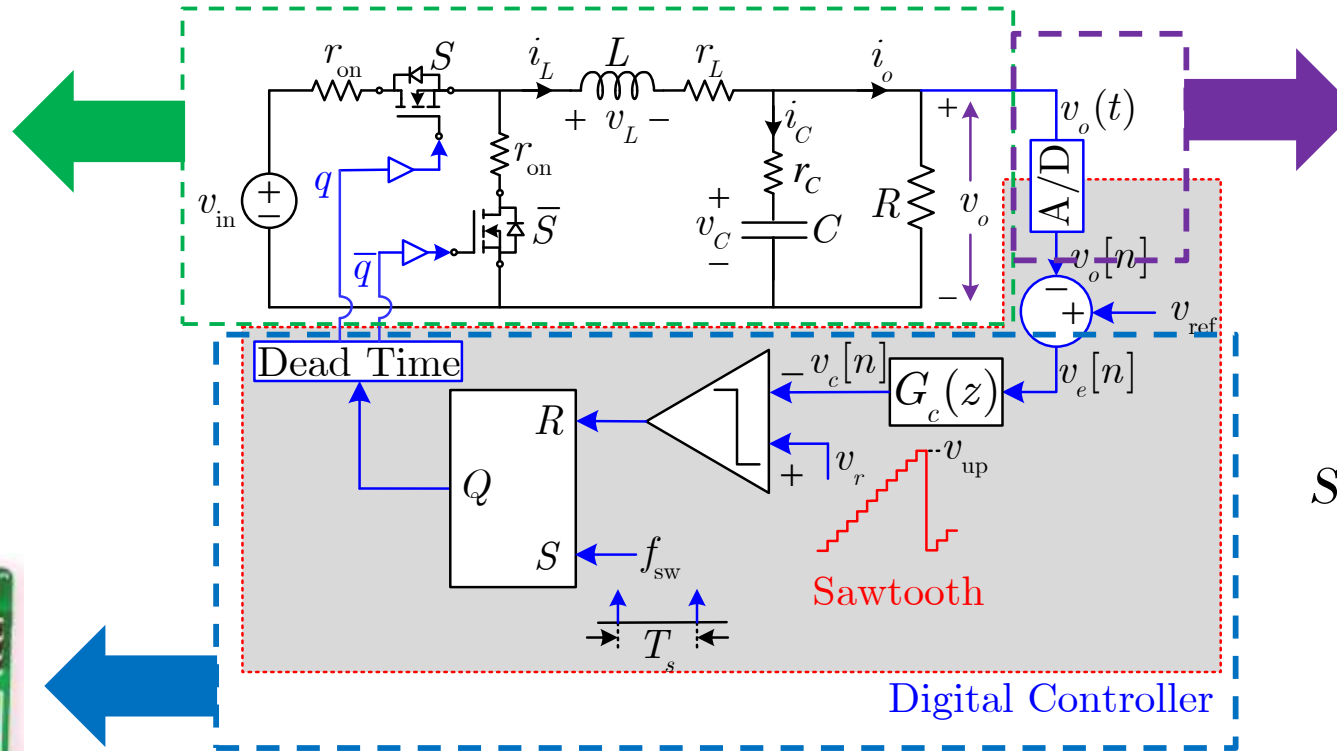
Digital Voltage Mode Control in a Buck Converter



Buck & Boost Converters



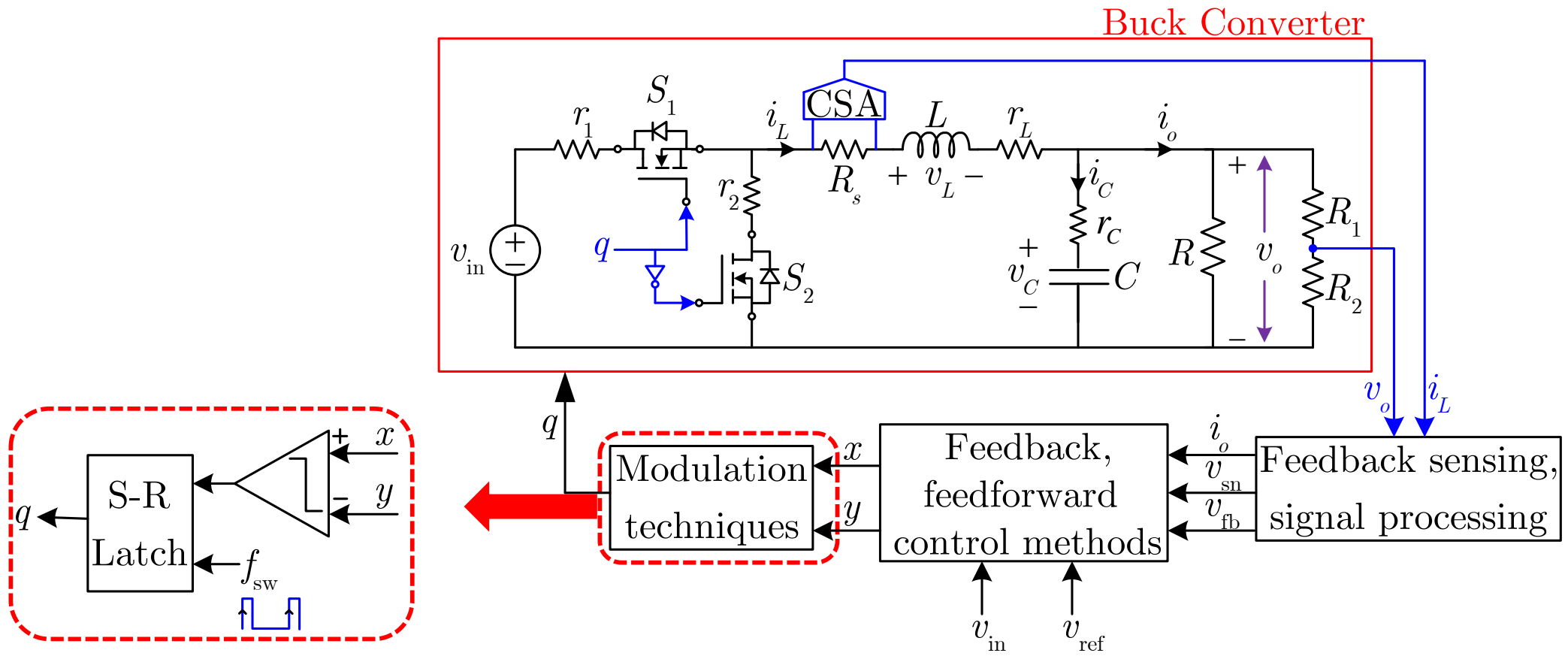
Xilinx FPGA kit



Signal conditioning board

NPTEL course on “Digital Control in Switched Mode Power Converters and FPGA-based Prototyping” on [YouTube](#)

Overview of Feedback/Feedforward Control Methods



S. Kapat & P. Krein, "A Tutorial and Review Discussions ...", *IEEE Open J. Power Electronics*, vol. 1, 2020



Overview of Control Methods

❑ **Output feedback control**

Voltage mode control – single loop

Current mode control – two loop

Ripple based control – single/two-loop

❑ **Feedforward control**

Input voltage/load current feedforward

DC droop control (AVP)

Small-signal linear control or large-signal nonlinear control – switching converters!!

❑ **State feedback control**

State feedback linear/nonlinear control

Observer based state feedback control

State feedback control – modulators

❑ **Fixed/variable frequency control**

Trailing/leading/double-edge modulator

Constant on/off-time, hysteresis control



Why Growing Emphasis on Digital Control?

- ❑ *Flexibility, portability, reconfigurability* – varying topologies, process technology, etc.
- ❑ *Digital communication & control* – reliable, fault-tolerant, smart power supply network
- ❑ *Hardware/software/firmware integration* – optimized solutions, third-party interface
- ❑ *Higher efficiency, lower component count, advanced control for faster transient*
- ❑ *Digital PMIC, digital control IC, digital control plug-and-play modules*
- ❑ *Rapid prototyping* – shorter technology & product development time

Lecture~01, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)



Challenges in Digital Control Commercial Products?

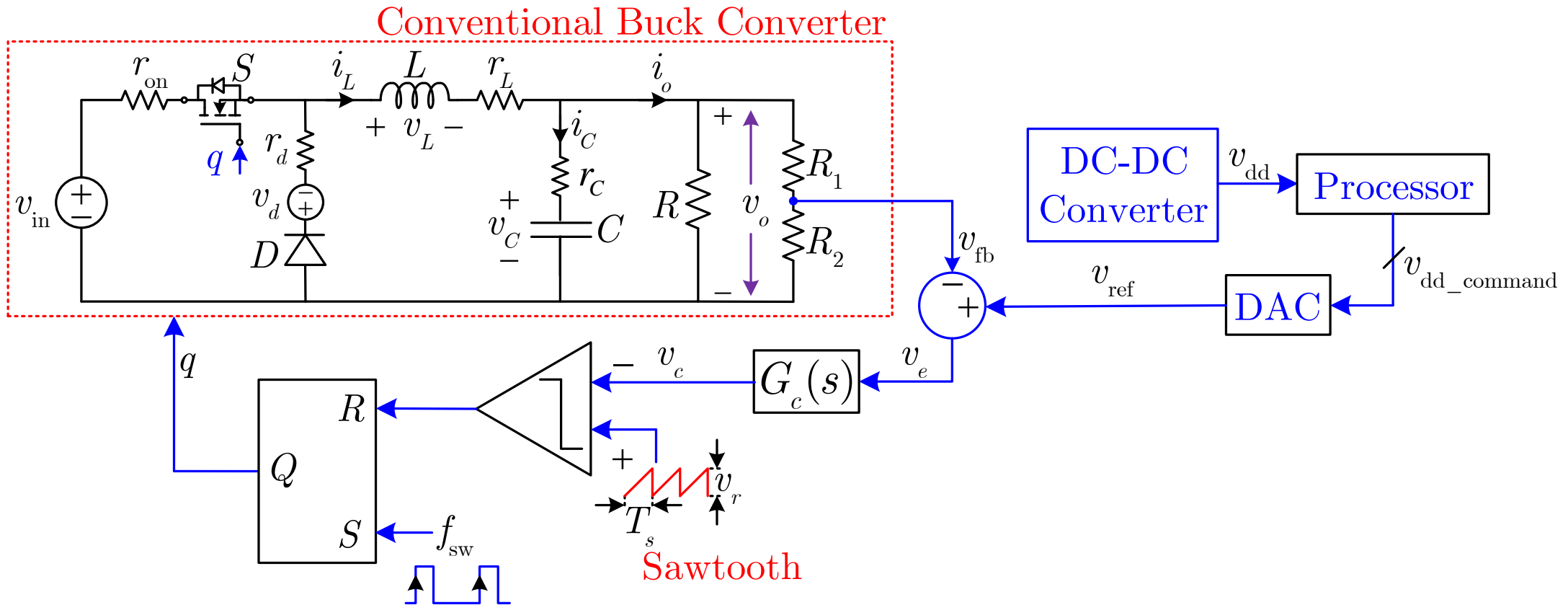
- ❑ *Cost* – ADC/DAC (bit size, conversion time), digital controller computation time
- ❑ *Level of digitization* – housekeeping to mixed-signal to fully digital solutions
- ❑ *Architecture* – modulation techniques, sampling methods, implementation platforms
- ❑ *Power consumption* – loop delay (sampling rate), voltage regulation (bit size)
- ❑ *Modeling, analysis and design methodology* – stability and performance
- ❑ *Mixed domain IP development* – FPGA prototyping to ASIC products

Lecture~01, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Step 1 of the Digitization Process in a Buck Converter

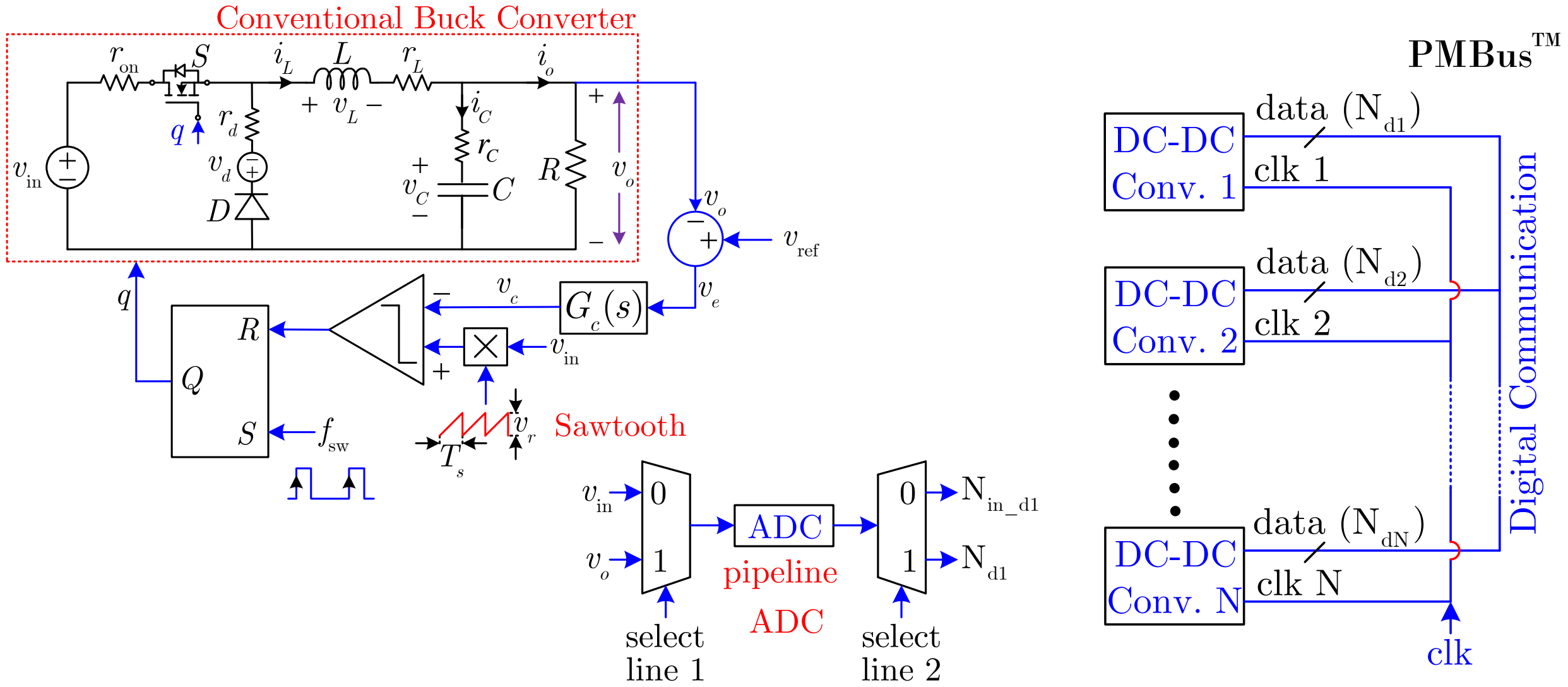
v_{ref} programming

- Dynamic adjustment of v_{ref} (maybe needed for DVS)



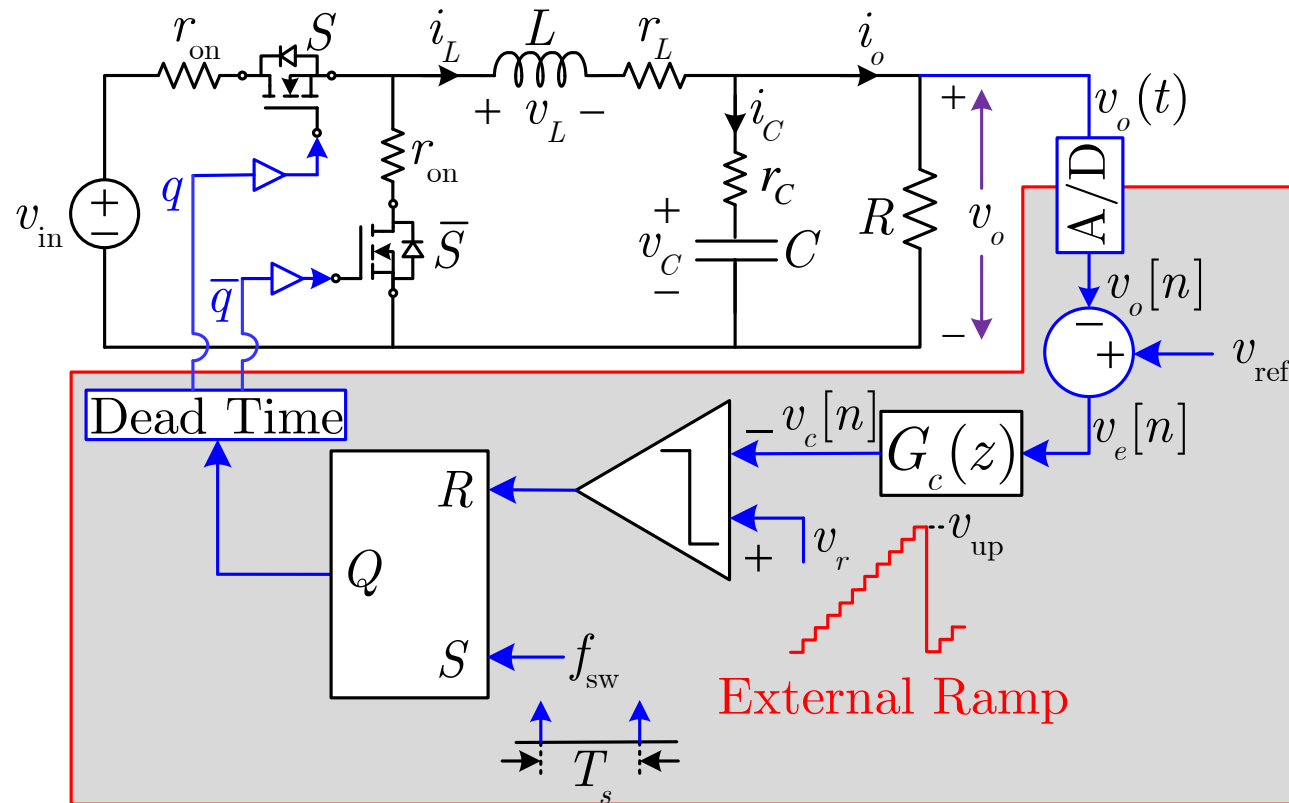
Lecture~05, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Step 2 of the Digitization Process in a Buck Converter

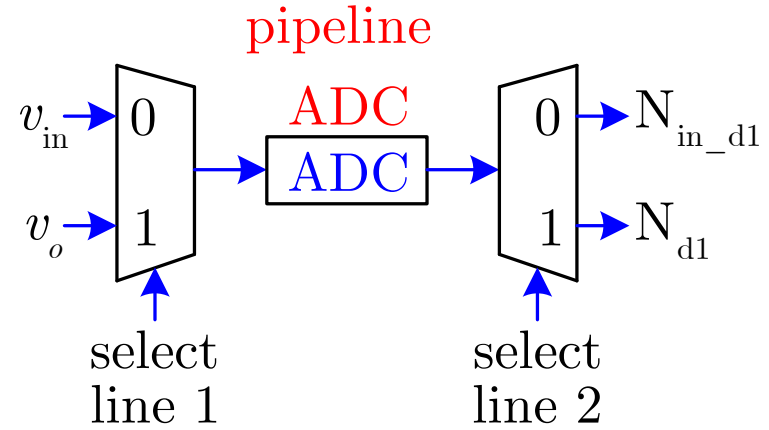


Lecture~05, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Step 3 of the Digitization Process – Digitizing Voltage Loop



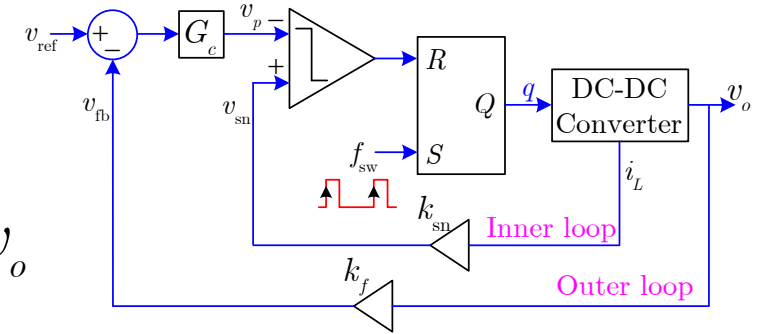
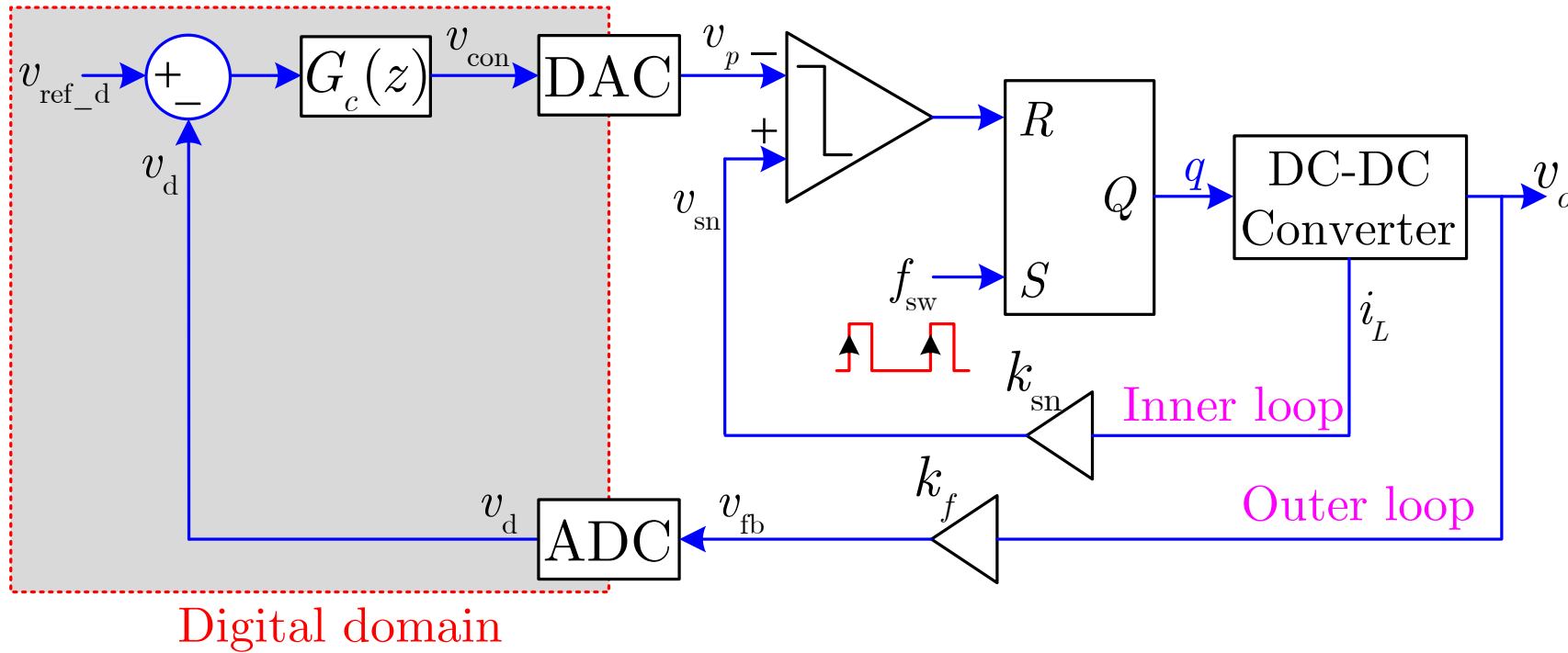
Digital Controller



Single-Loop Digital Voltage Mode Control

Lecture~08, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Step 4 – Digitizing Voltage Loop in Digital CMC



- Current feedback in analog domain
- Voltage feedback in digital domain

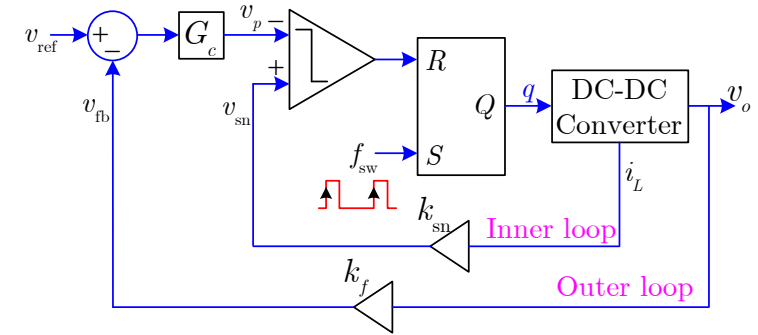
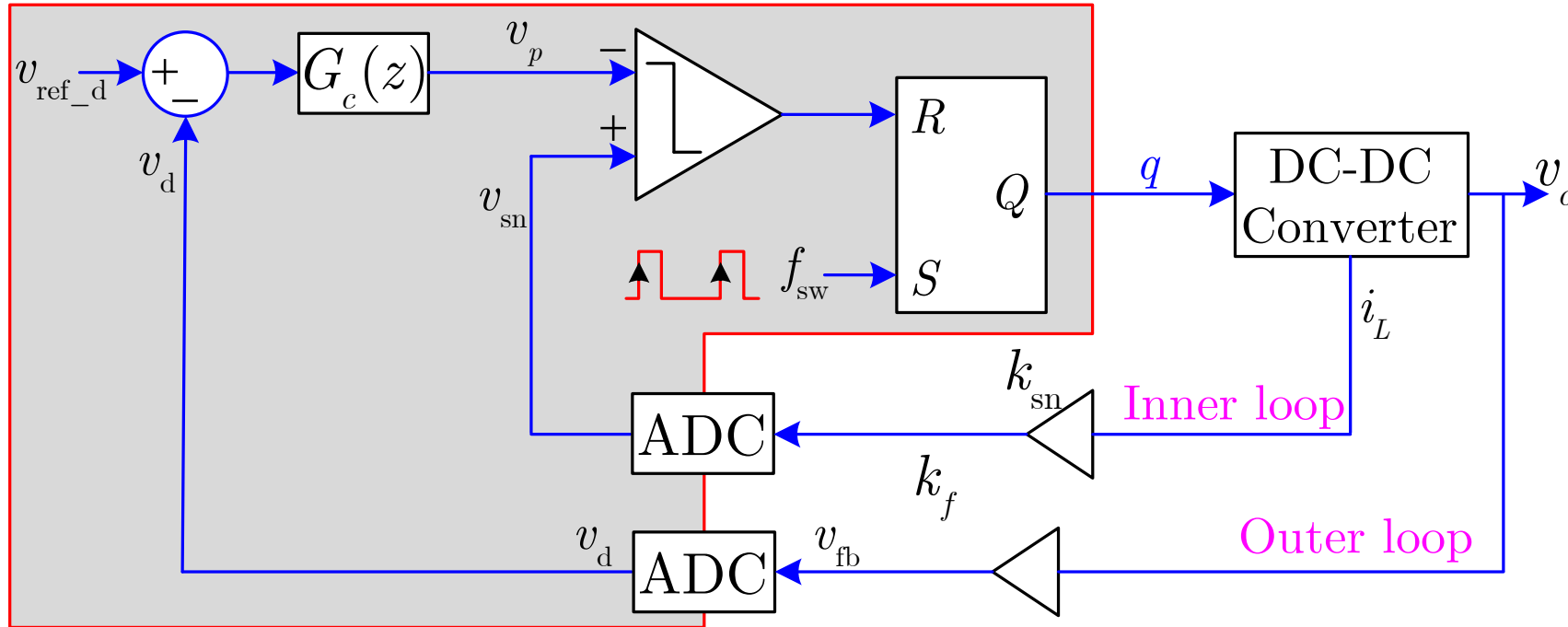
Digital of CMC: Architecture - I

Mixed-signal CMC

Lecture~09, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)



Step 5 – Digitizing both Voltage & Current Loops in Digital CMC



Digital Implementation

- Both current and voltage feedback loops in the digital domain

Digital of CMC: Architecture -II

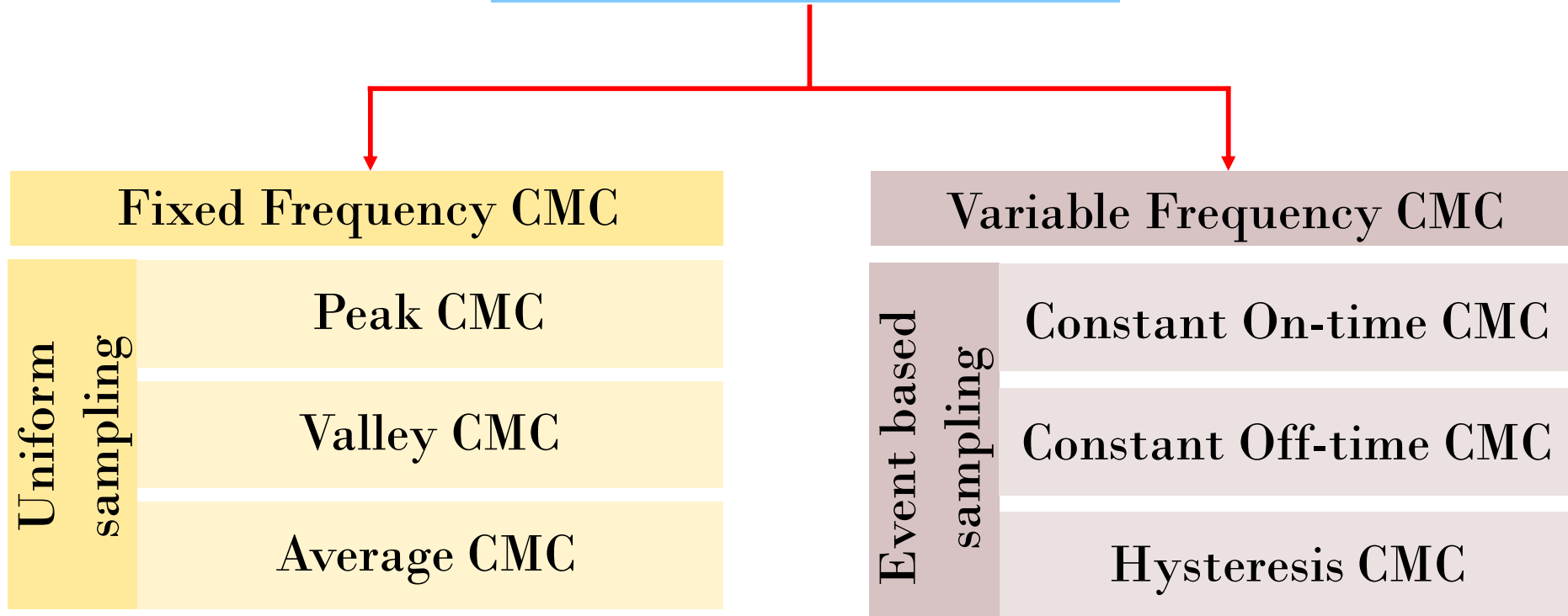
Fully digital CMC

Lecture~09, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)



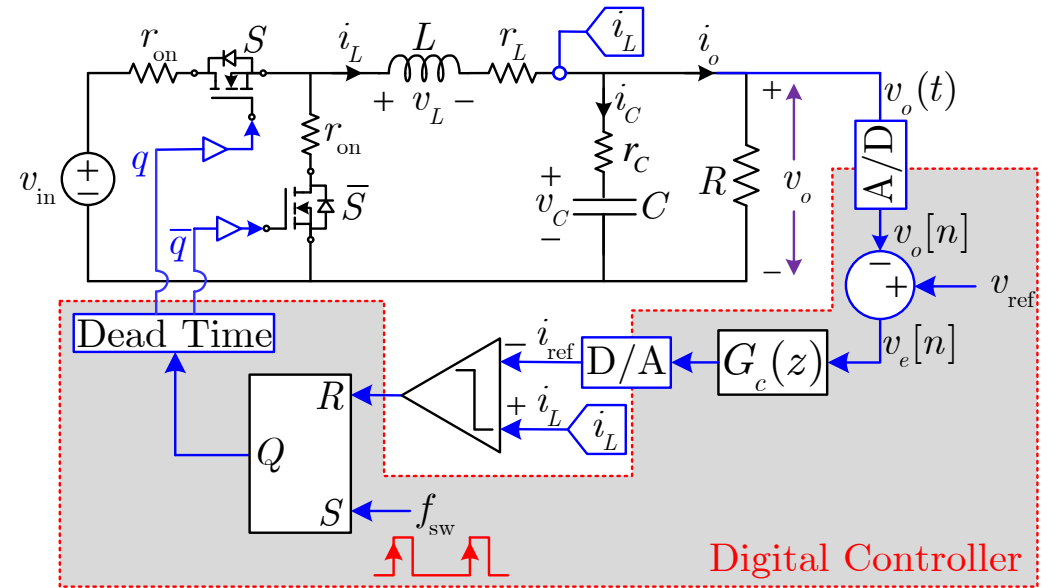
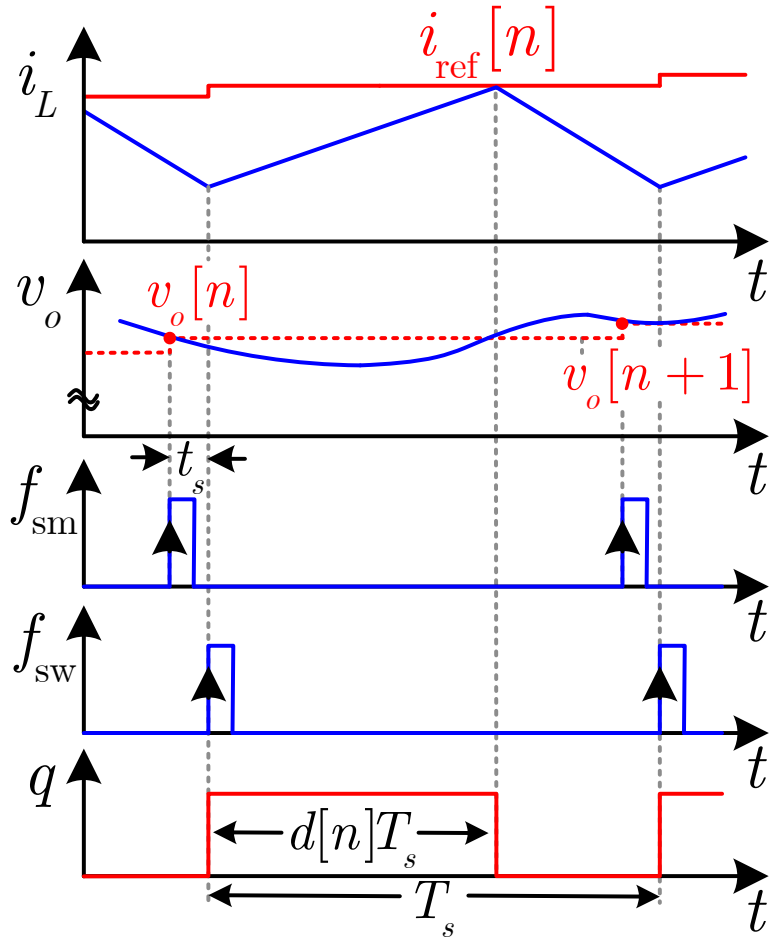
Digital Current Mode Control Architectures

Digital CMC Architectures



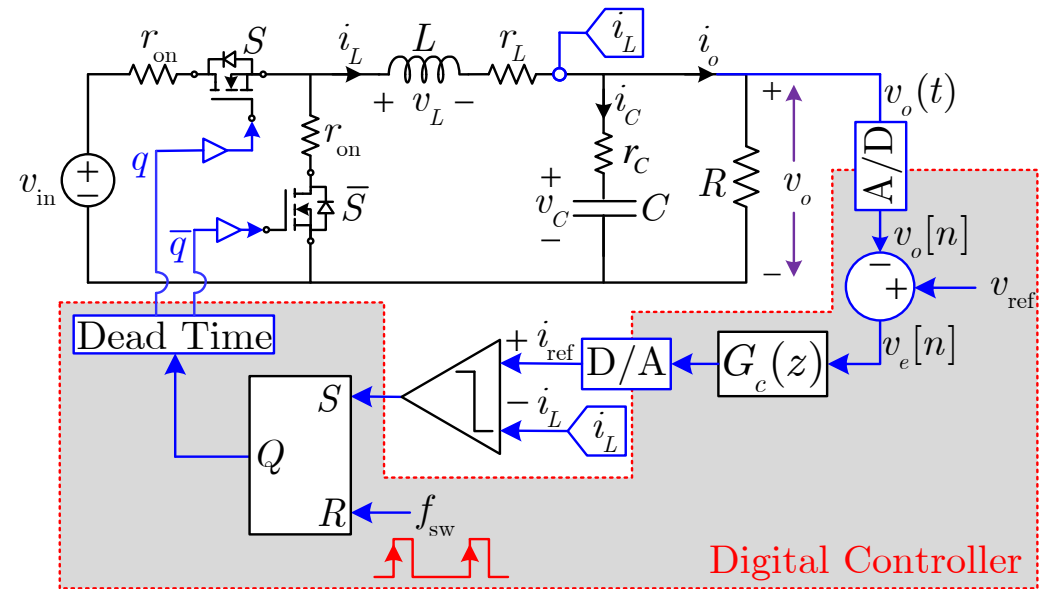
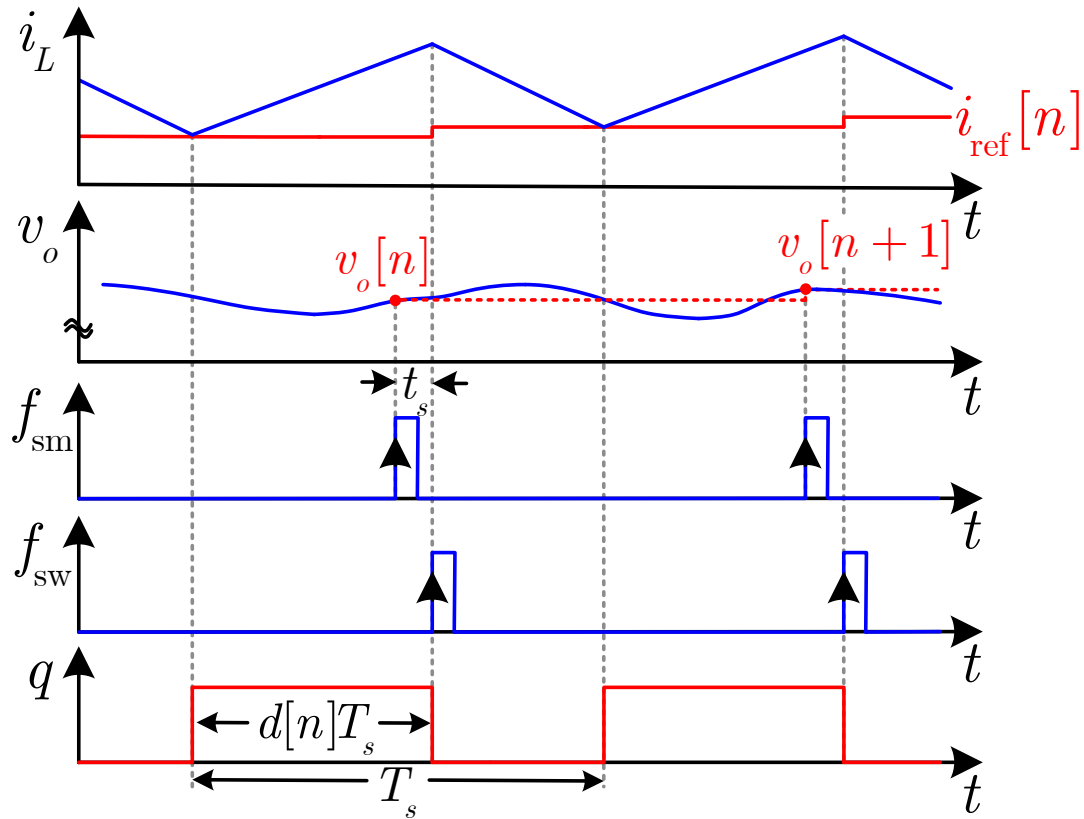
Lecture~20, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Mixed-Signal Peak CMC Architecture



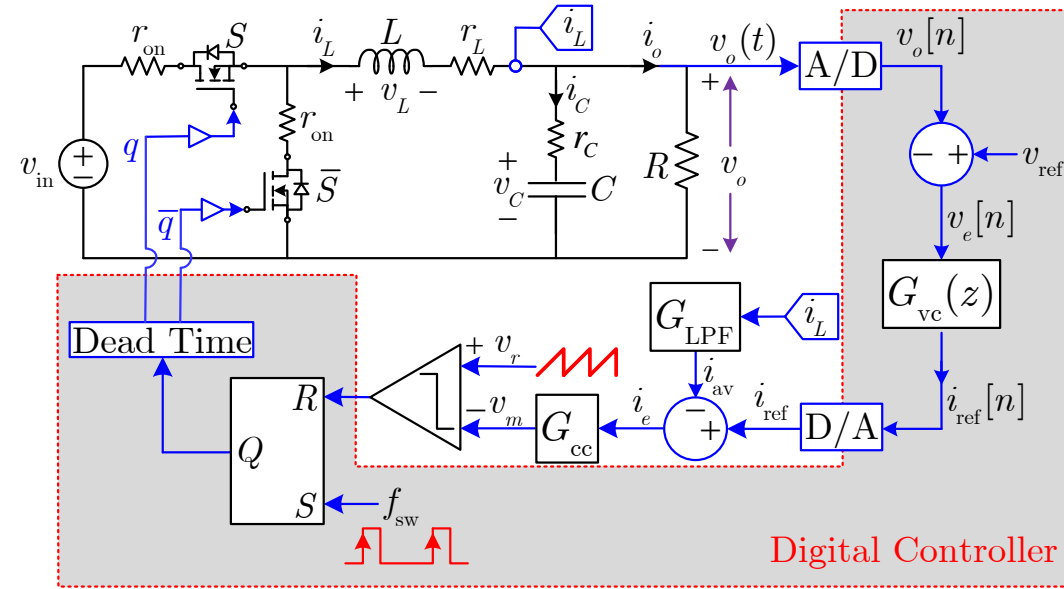
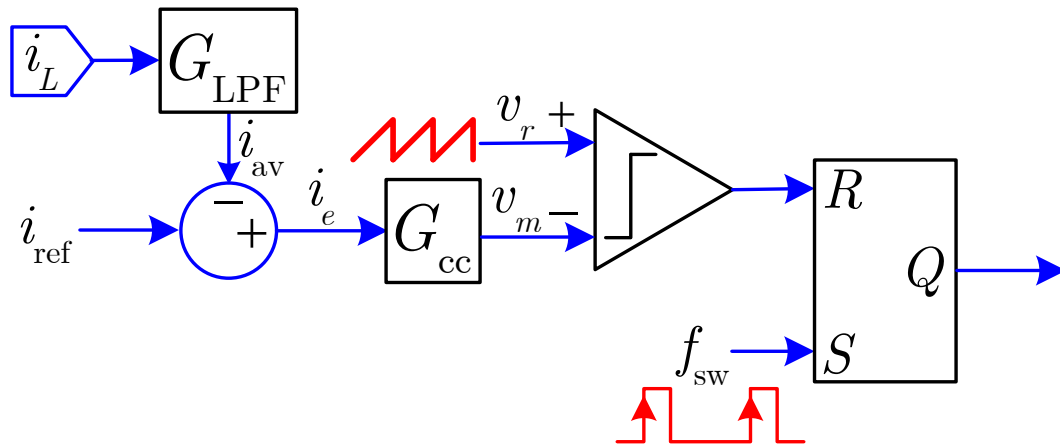
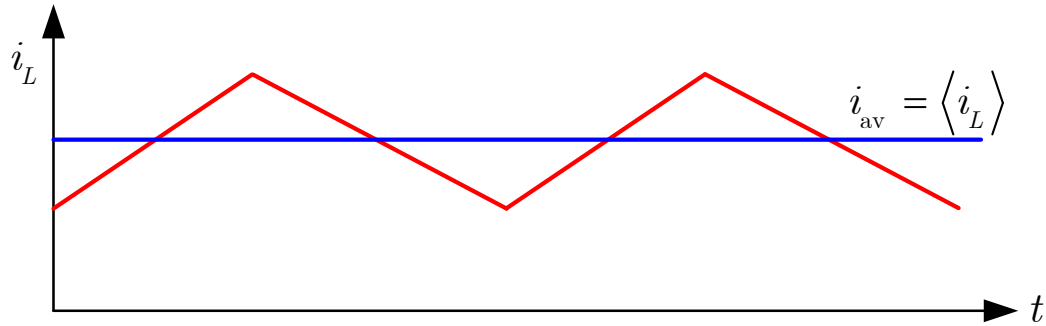
Lecture~15, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Mixed-Signal Valley CMC Architecture



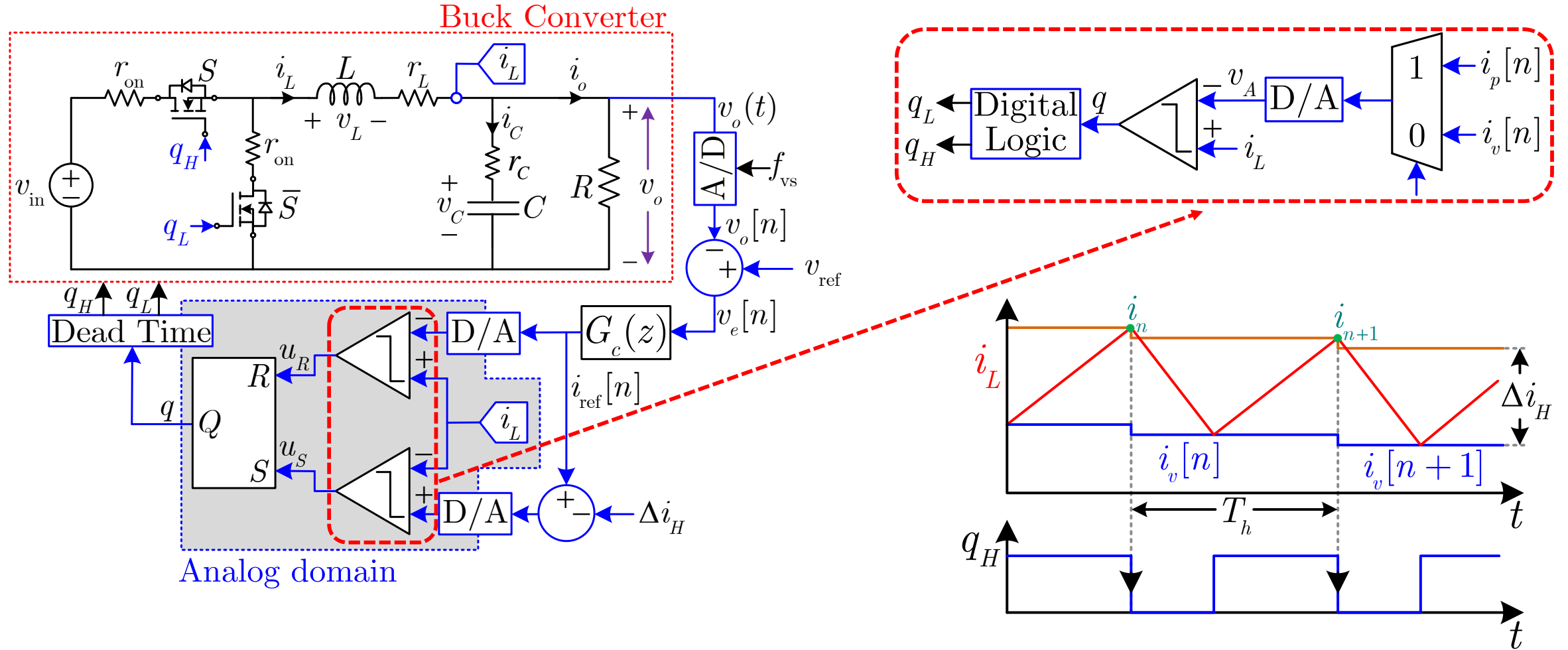
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Mixed-Signal Average CMC Architecture



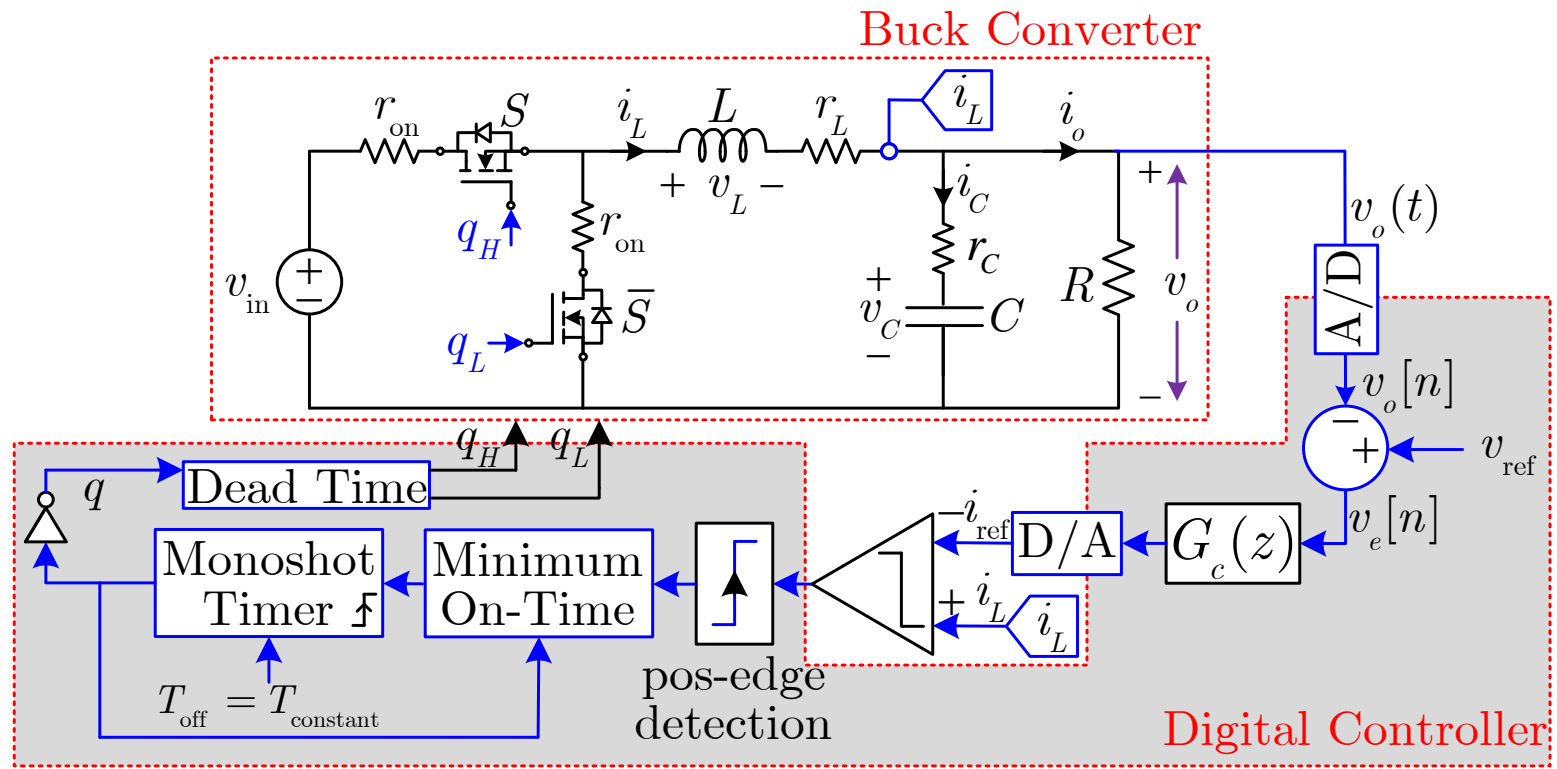
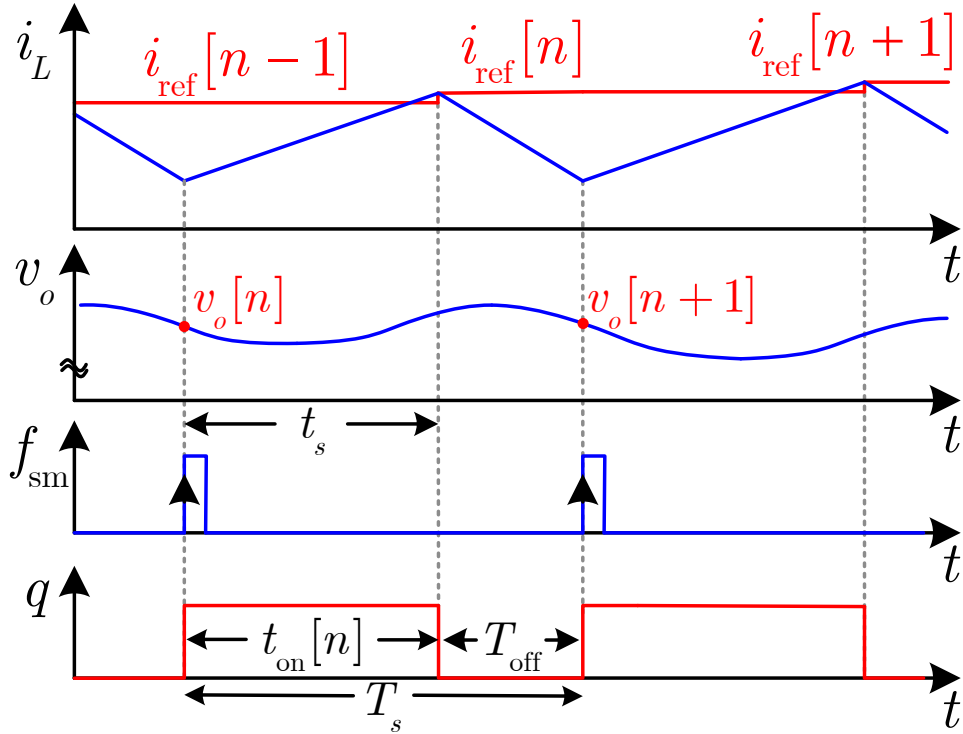
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Mixed-Signal Hysteresis Current Control Architecture



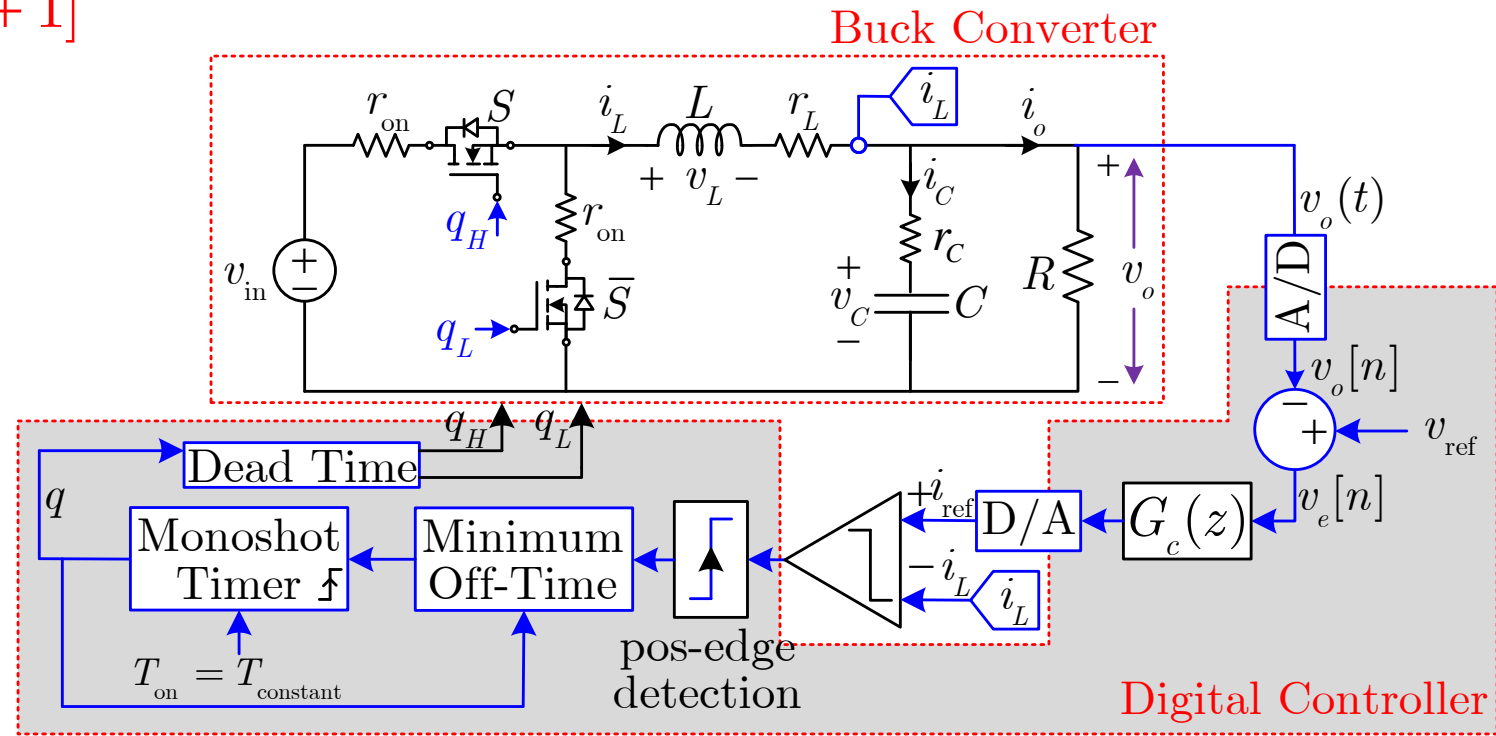
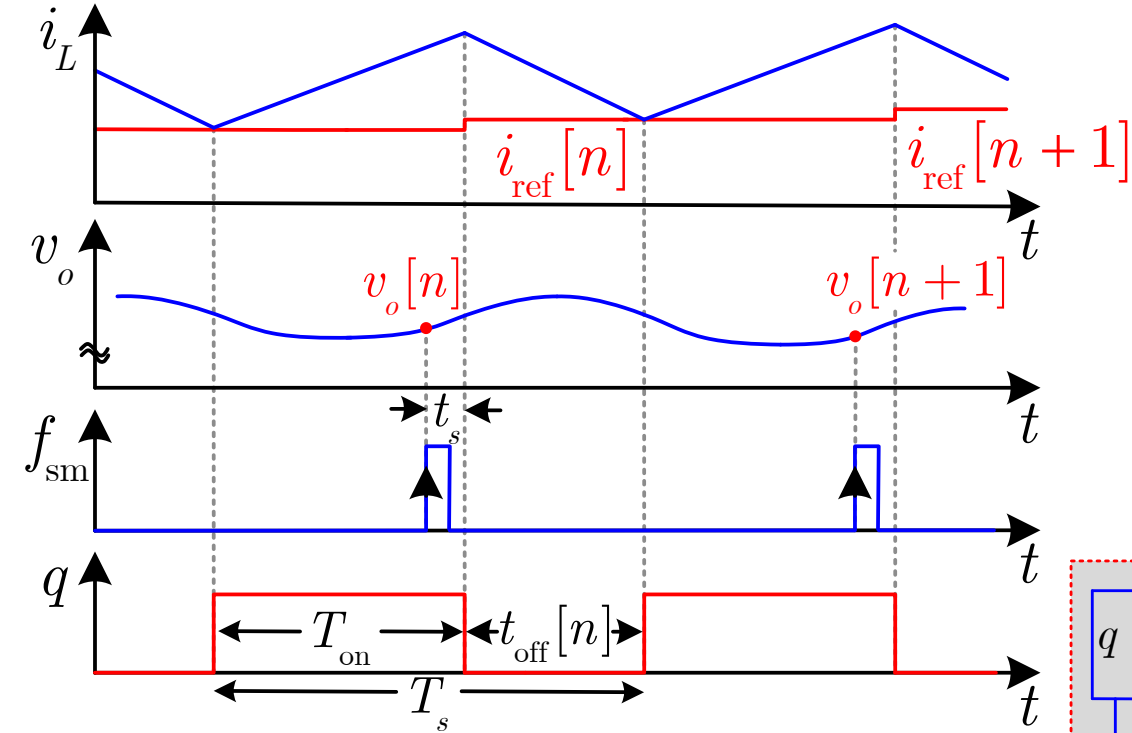
Lecture~19, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Mixed-Signal Constant Off-time Peak Current Mode Control



Lecture~17, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Mixed-Signal Constant On-time Current Mode Control

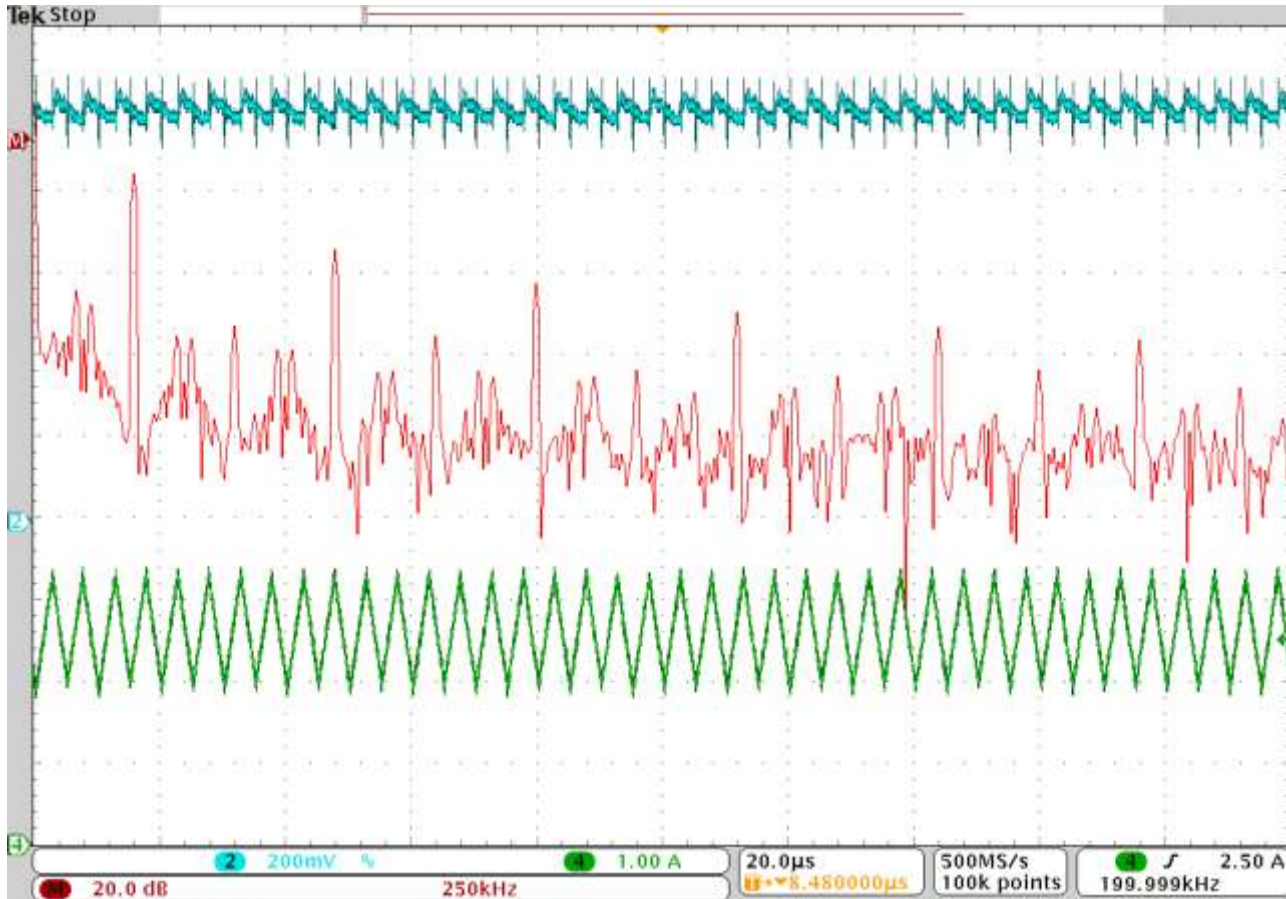


Lecture~17, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

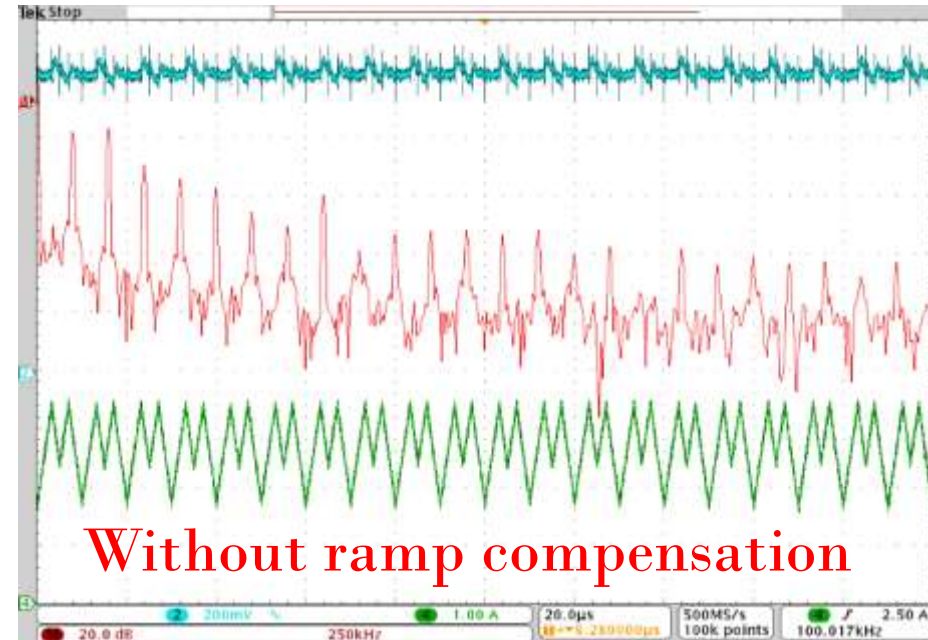
Stabilizing Current Loop in Fixed-Frequency Digital CMC

Operating Conditions

Input Voltage V_{in}	2.2 V
Load Resistance R	0.32 Ω
Current Reference I_{ref}	3.4 A
Switching Frequency f_{sw}	200kHz



With ramp compensation

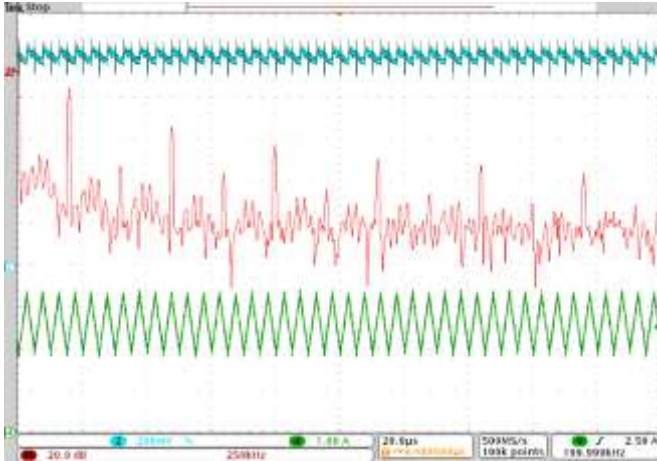


Without ramp compensation

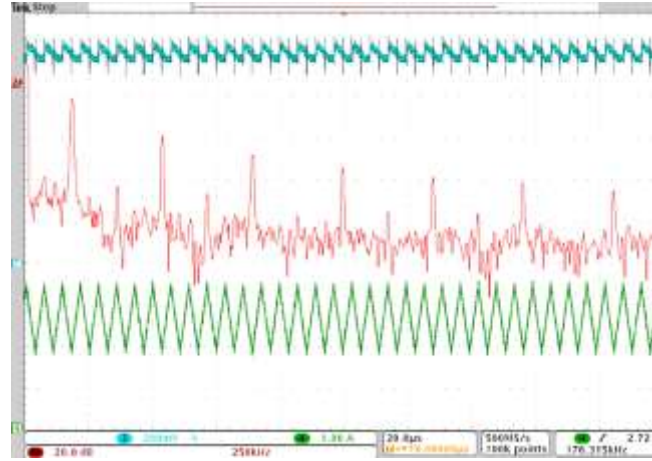
Lecture~93, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Experimental Results – A Comparative study

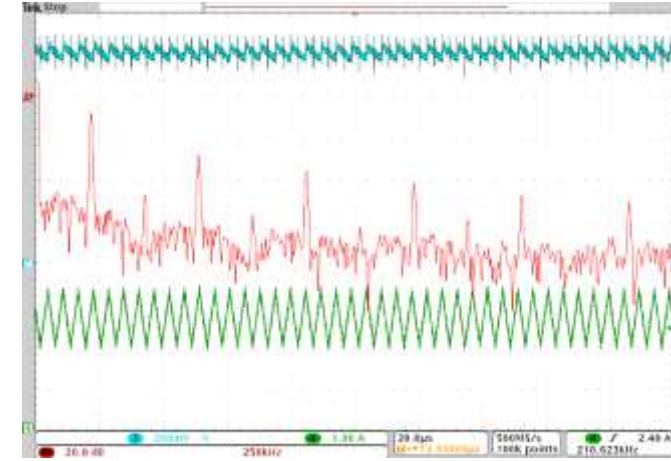
Peak CMC with ramp



Constant off-time peak CMC



Constant on-time valley CMC



Operating Conditions

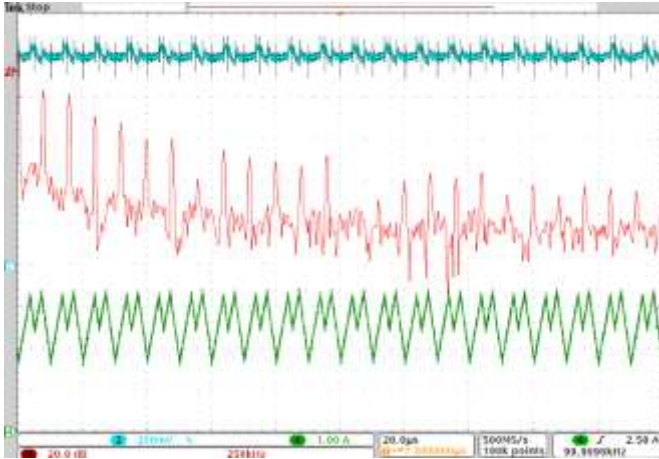
Input Voltage V_{in}	2.25 V
Load Resistance R	0.32 Ω
Current Reference I_{ref}	3.4 A / 2 A

- Constant on/off-time DCMC – current loop inherently stable without ramp compensation
- **Fixed-freq. DCMC requires ramp compensation**

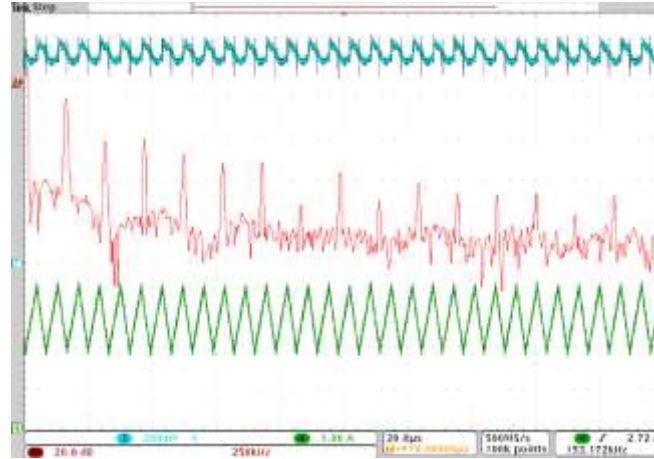
Lecture~98, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Experimental Results – A Comparative study

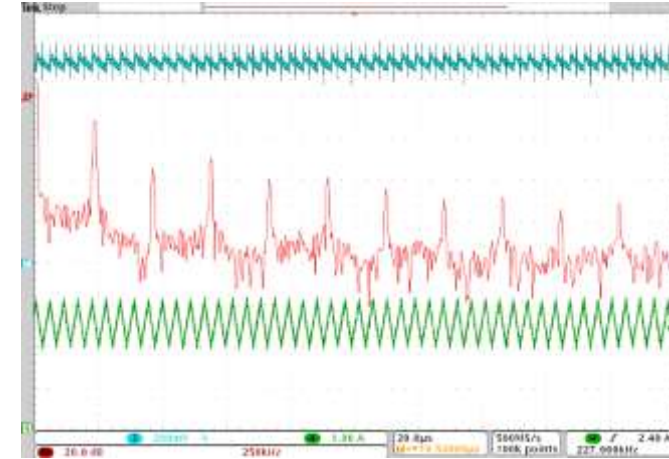
Peak CMC with ramp



Constant off-time peak CMC



Constant on-time valley CMC



Operating Conditions

Input Voltage V_{in}	2 V
Load Resistance R	0.32 Ω
Current Reference I_{ref}	3.4 A / 2 A

- Constant on/off-time DCMC – current loop inherently, but varying switching frequency
- **Fixed-freq. DCMC – more ramp is required!!**

Lecture~98, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Comparative Study of Switching Frequency – CCM Buck Converter



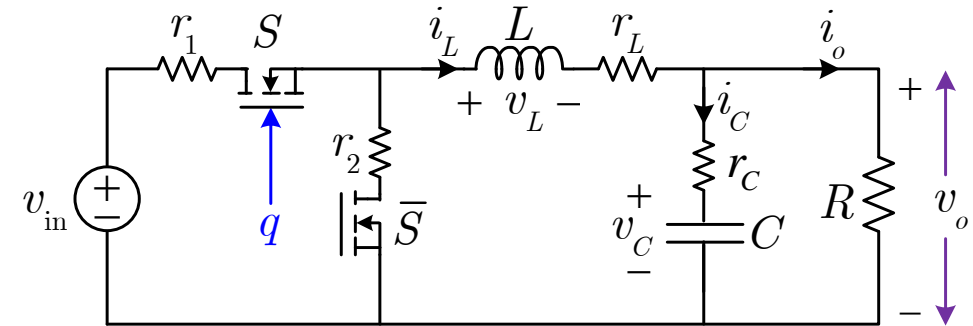
CMC Technique	Switching frequency (f_{sw})	Worst case scenario
Fixed frequency CMC	$f_{sw} = f_{ext}$	Insensitive to system and operating conditions
Constant on-time CMC	$f_{sw} = \frac{1}{T_{on}} \times \left(\frac{V_o}{V_{in}} \right)$	Highest switching frequency at lowest input voltage
Constant off-time CMC	$f_{sw} = \frac{1}{T_{off}} \times \left(1 - \frac{V_o}{V_{in}} \right)$	Highest switching frequency at highest input voltage

Lecture~98, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Digital Control – Modeling Techniques for Analysis and Design

Buck Converter – Continuous-time (CT) Control-to-Output TF

$$G_{vd}(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{V_{IN}}{R + r_e} \frac{1 + r_c C s}{R \left(1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2} \right)}$$



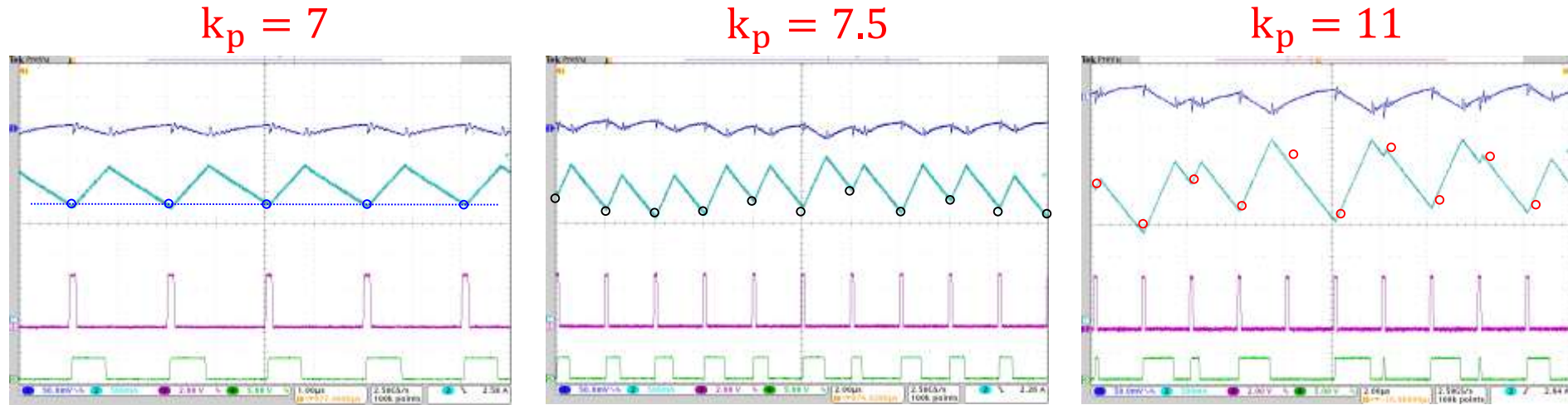
$$G_{vd_delay}(s) = \left(\frac{V_{IN}}{R + r_e} \right) \frac{1 + r_c C s}{R \left(1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2} \right)} \times e^{-s\tau_d}$$

Total loop delay $\tau_d = t_s + DT$

- Continuous-time (CT) small-signal model (SSM) with delay—insightful
- Suitable for design up to freq. $\frac{f_{sw}}{10}$
- **Fail to predict fast-scale instability!!**

Lecture~31, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

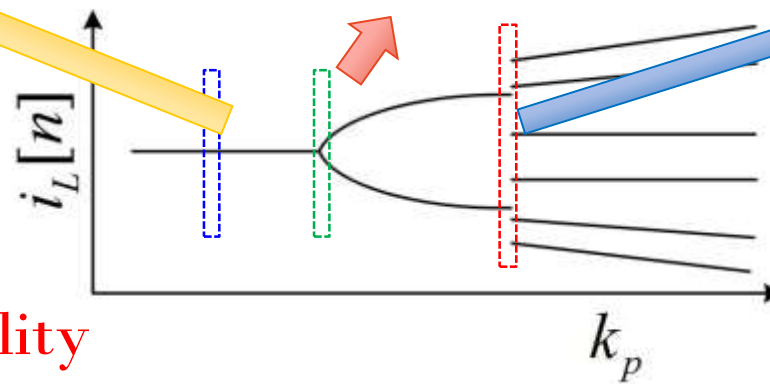
Instability due to Sampling Delay in Digital Current Mode Control



Period-1 orbit

Smooth bifurcation

Non-smooth bifurcation

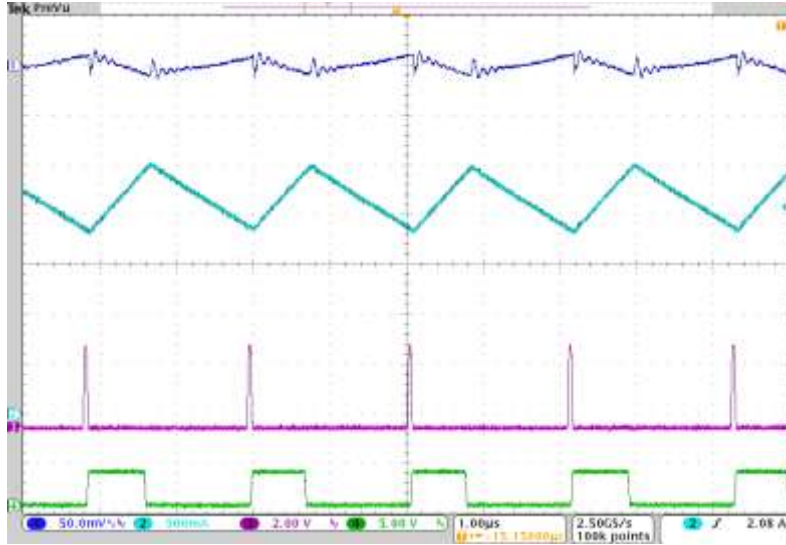


- Digital CMC with $D < 0.5$
- CT SSM fails to capture instability
- Identified root cause of border collision bifurcation

[S. Kapat, "Fixed and Variable Frequency Digital Current Mode Control...", APEC 2021]

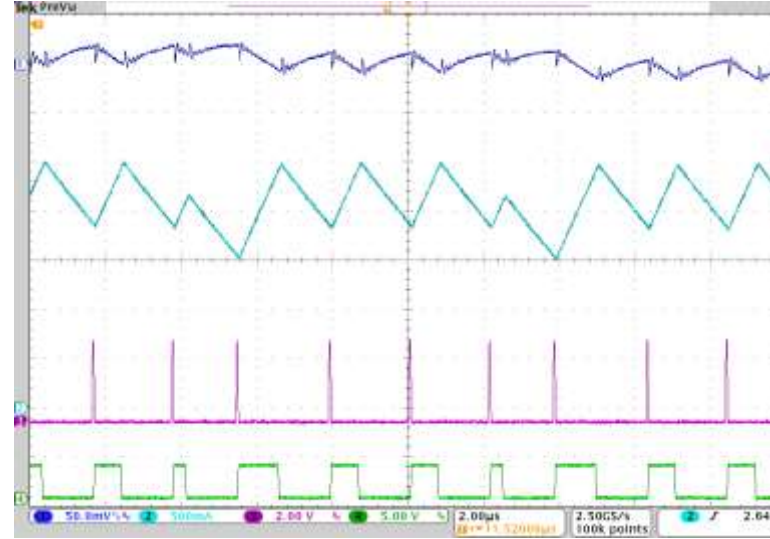
Event-based Constant Off-Time Digital CMC Boost Converter

$k_p = 7$



Event-based sampling – stable

$k_p = 12$



Event-based sampling – instability

$v_{in} = 3.3 \text{ V},$
 $v_o = 5 \text{ V},$
 $i_o = 1.5 \text{ A},$
 $f_{sw} = 500 \text{ kHz}$
 $k_i = 0.015$

- Constant off-time exhibits smooth bifurcation only
- Ripple & RMS quantities would be smaller compared to DPWM
- Inherent current-loop stability and fast transient performance

[S. Kapat, “Fixed and Variable Frequency Digital Current Mode Control...”, APEC 2021]

Digital Control – Modeling Techniques for Analysis and Design

Buck Converter – Discrete-time (DT) Control-to-Output TF

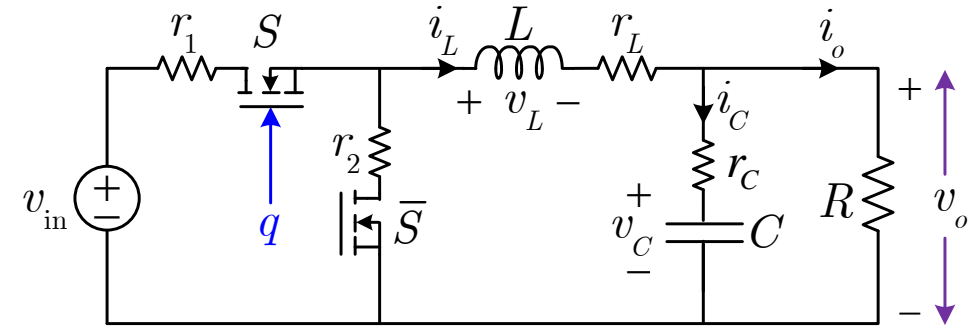
$$\tilde{x}_{n+1} = A_{\text{eq}} \tilde{x}_n + B_{\text{eq}} \tilde{d} \quad \text{and} \quad \tilde{v}_o[n] = C_{\text{eq}} \tilde{x}_n$$

where $A_{\text{eq}} = e^{AT}$ and $B_{\text{eq}} = e^{A(T-t_d)} B_1 V_{\text{in}} T$

$$C_{\text{eq}} = \begin{bmatrix} \alpha r_C & \alpha \end{bmatrix}$$

$$G_{\text{vd}}(z) = \frac{\tilde{v}_o(z)}{\tilde{d}(z)} = C_{\text{eq}} (zI - A_{\text{eq}})^{-1} B_{\text{eq}}$$

total loop delay $\tau_d = t_s + DT$



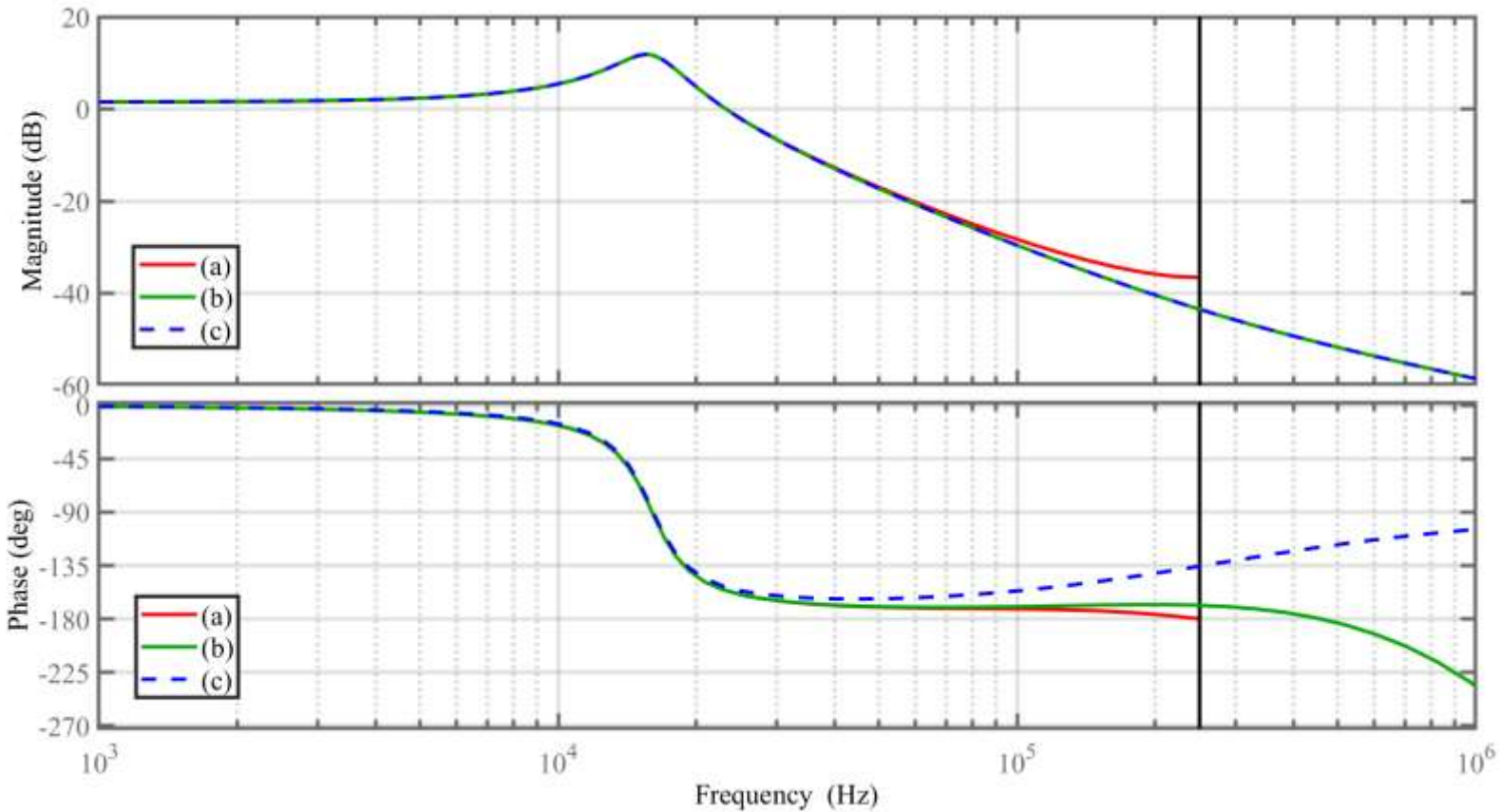
- Discrete-time (DT) SSM – capable of accurately predicting fast-scale instability
- Suitable for design up to freq. $\frac{f_{sw}}{2}$
- **Complex expression – no circuit insight!!**

Lecture~38, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)



Digital Control – Modeling Techniques for Analysis and Design

(a) DT SSM $G_{vc}(z)$, (b) CT SSM $G_{vc_delay}(s)$ with delay $\tau_d = t_s + DT$, (c) CT SSM $G_{vc}(s)$



- CT SSM – simple, but not sufficient to ensure stability
- DT SSM – accurate, but does not offer circuit insight
- A combined CT/DT approach for digital controller design

Lecture~40, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)



Design of Digital VMC Boost Converter – Freq. Domain Approach

Step 1: Select gain crossover frequency ω_c by setting $k = \frac{1}{5}$ $\omega_c = k \times \omega_{rhp}, \quad k < 1$

Step 2: Compute phase margin (PM) $PM = 90^\circ - \tan^{-1} \left(\frac{2\omega_n}{1 - \omega_n^2} \right) \Big|_{\omega_n = \frac{\omega_c}{\omega_{rhp}}} - \omega_c \tau_d$

Step 3: For given τ_d , verify whether PM meets the requirement, typically $PM > 45^\circ$

Step 4: If not, go to step~1, reduce k and repeat the process till PM is met

Step 5: If step~3 is passed, find $K_i = \frac{\omega_c (1 - D)^2}{F_m V_{in}}$

Step 6: Verify fast-scale stability using discrete-time small-signal models (refer to Lecture~39)

Lecture~43, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Design of Digital CMC Boost Converter – Freq. Domain Approach



Step 1: Select gain crossover frequency ω_c by setting $k = \frac{1}{3}$ $\omega_c = k \times \omega_{rhp}, \quad k < 1$

Step 2: Compute phase margin (PM) $PM = 90^\circ - \tan^{-1} \left(\frac{2\omega_n}{1 - \omega_n^2} \right) \Big|_{\omega_n = \frac{\omega_c}{\omega_{rhp}}} - \omega_c \tau_d$

Step 3: For given τ_d , verify whether PM meets the requirement, typically $PM > 45^\circ$

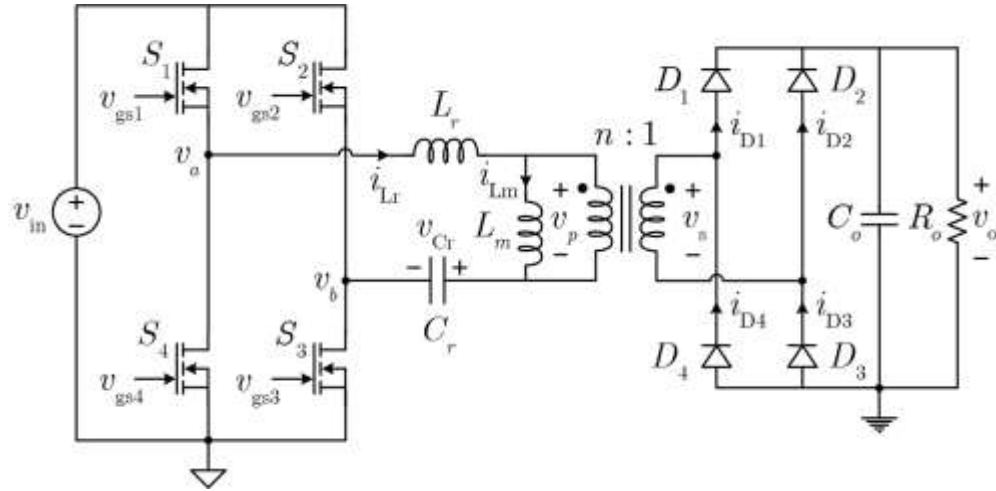
Step 4: If not, go to step~1, reduce k and repeat the process till PM is met

Step 5: If step~3 is passed, find $K_c = \frac{2\omega_c(1-D)}{R}$

Step 6: Verify fast-scale stability using discrete-time small-signal models (refer to Lecture~39)

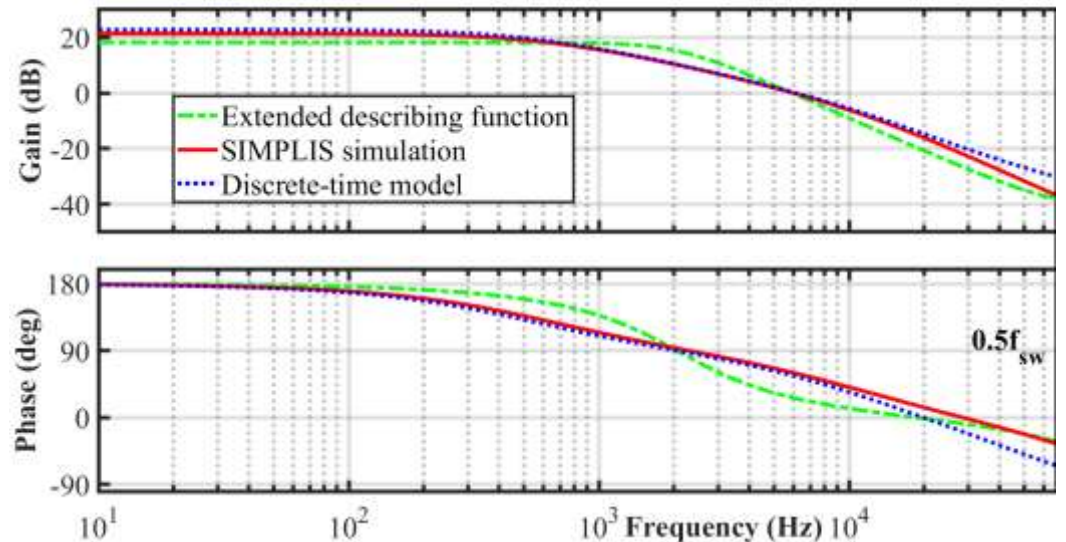
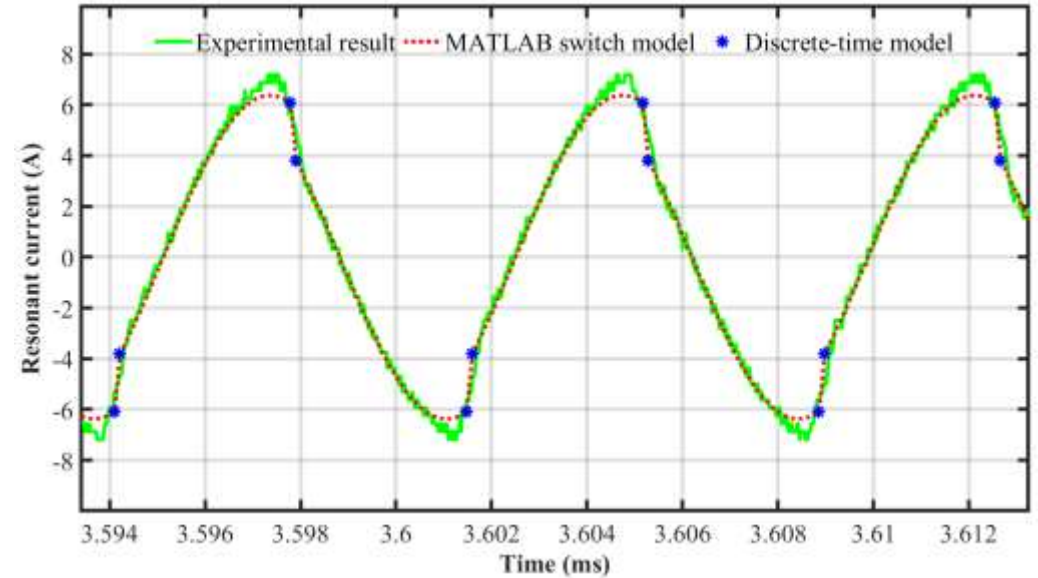
Lecture~43, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Discrete-Time Modeling Framework for Analysis of LLC Converter



- ❑ Unified Discrete-time modeling framework
- ❑ DT large/small-signal models – accurate and superior over Extended DF method

*IIT Kharagpur and
STMicroelectronics
Collaborative Research Work*

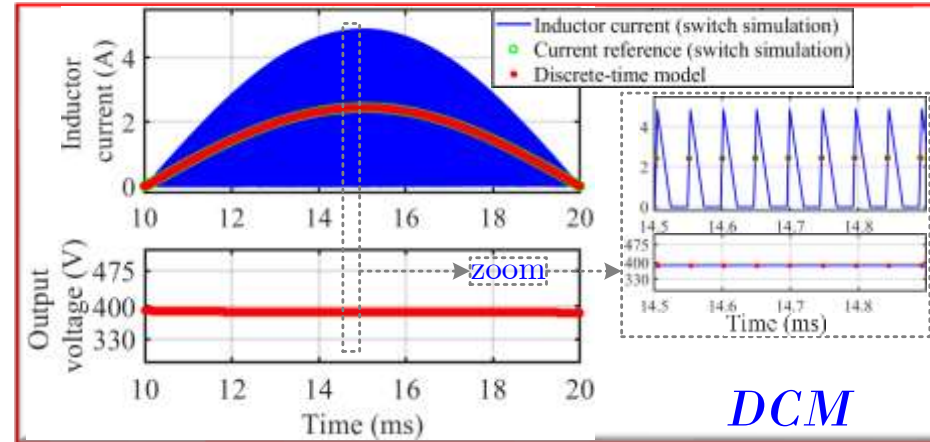
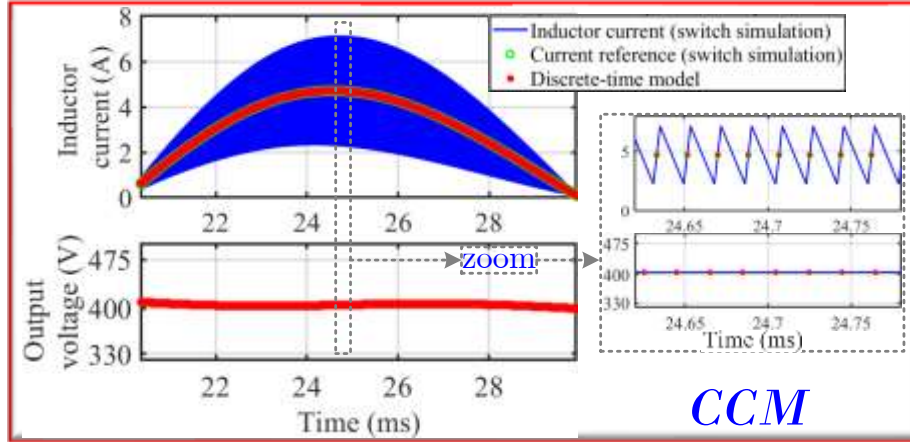


[G. R. Chilukuri, et. Al., "Discrete-Time Modeling Framework for Analysis ...", in proc. *IEEE APEC* 2022]

Unified DT Modelling of Digitally Controlled Boost PFC

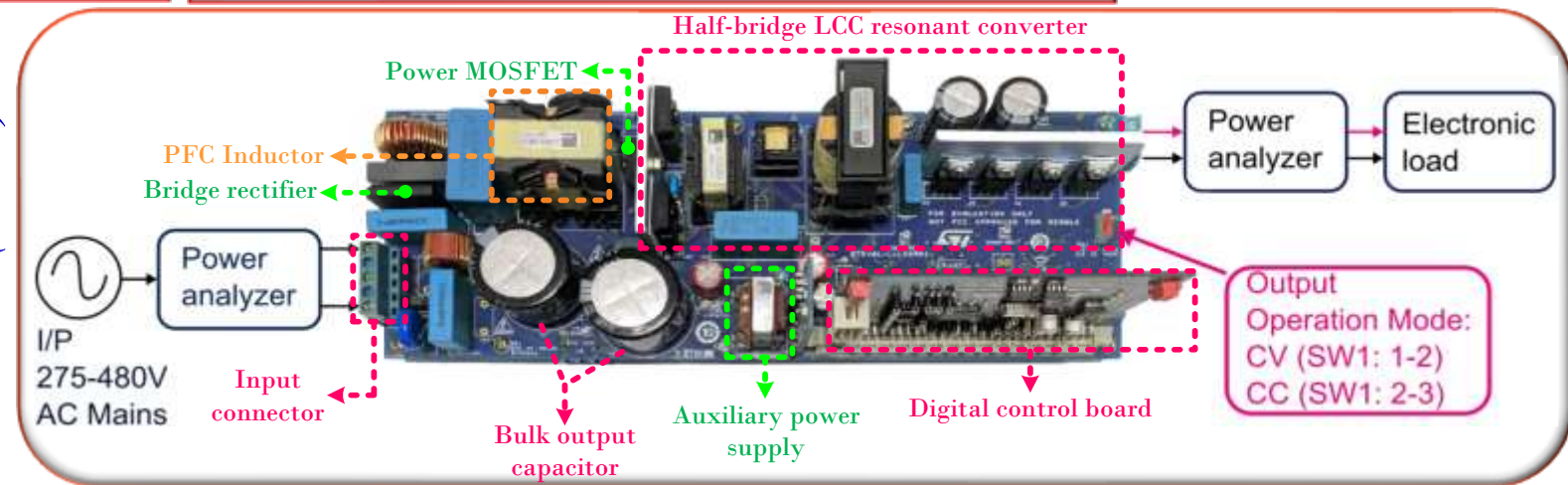
- Unified DT modeling framework – fixed/variable freq. digital control, CCM, CrM, DCM
- Digital controller design along with first-scale stability analysis using DT small-signal model

Large-signal model validation



IIT Kharagpur and STMicroelectronics Collaborative Research Work

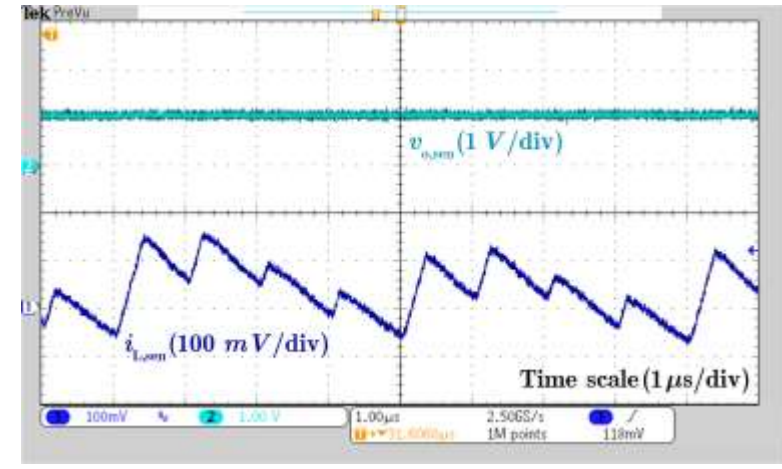
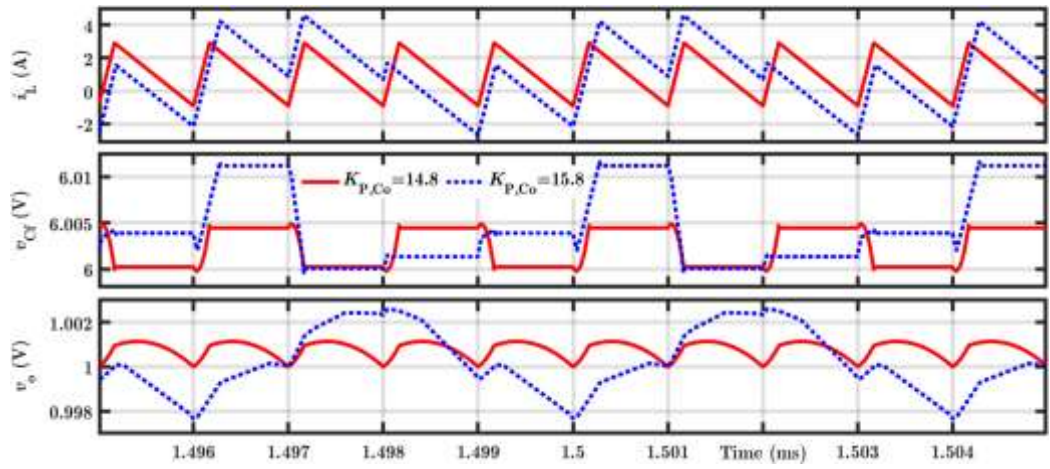
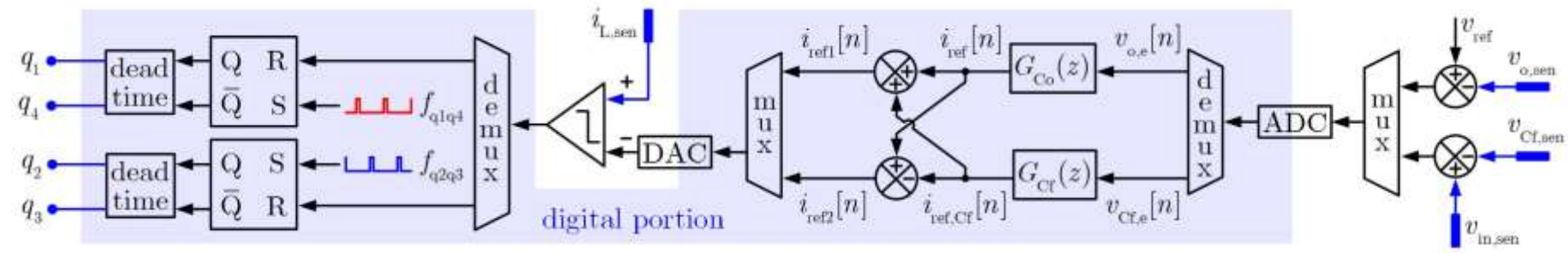
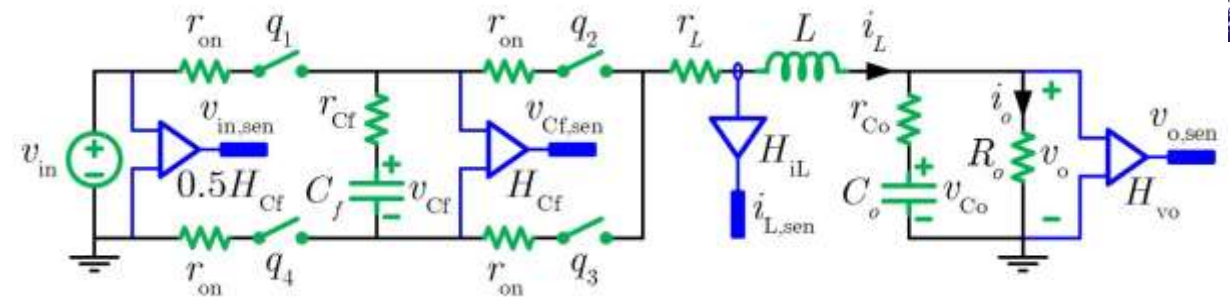
300 W very high AC input voltage LED driver (Link)



[D. Chatterjee, et al., “Unified Discrete-Time Large/Small-Signal Modeling...”, 2nd Best Paper, IEEE ONCON 2022]

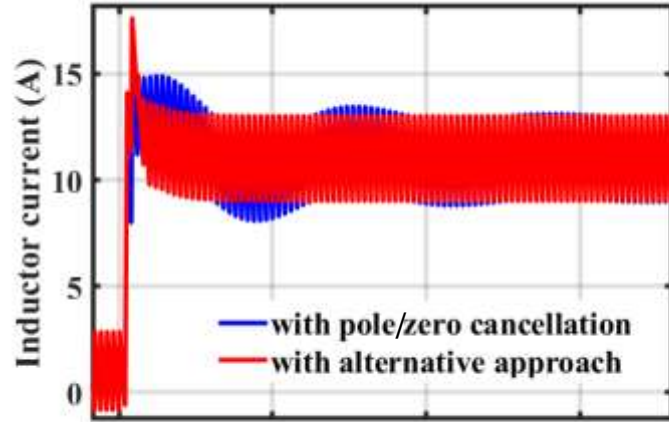
Closed-Loop Stability of PCMC Three Level Buck Converter

- ❑ Simplified discrete-time modeling
- ❑ Peak CMC active voltage balance
- ❑ Stability analysis of PCMC

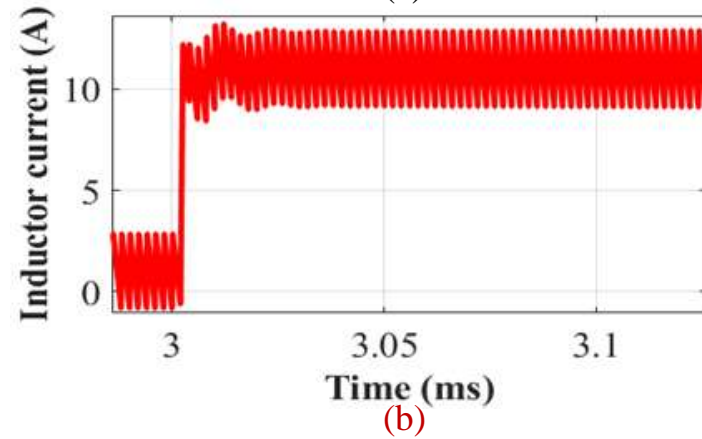


[G. R. Chilukuri, et. Al., "Closed-Loop Stability Analysis of Digitally Current ...", accepted, IEEE APEC 2023]

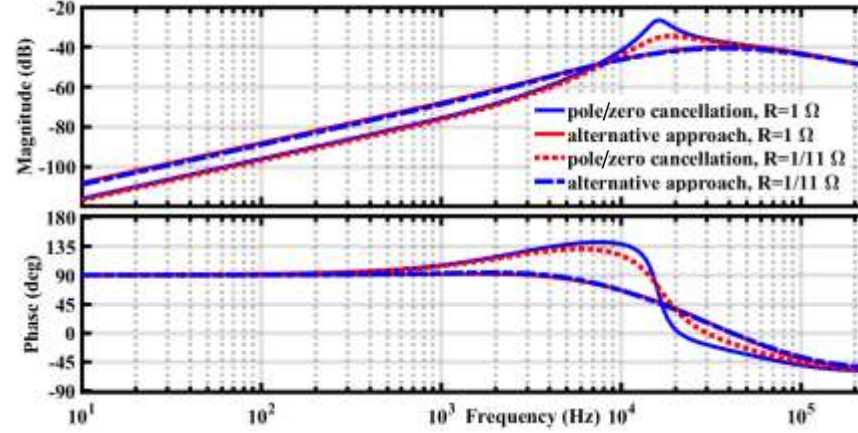
Design of Digital VMC & Digital CMC in DC-DC Converters



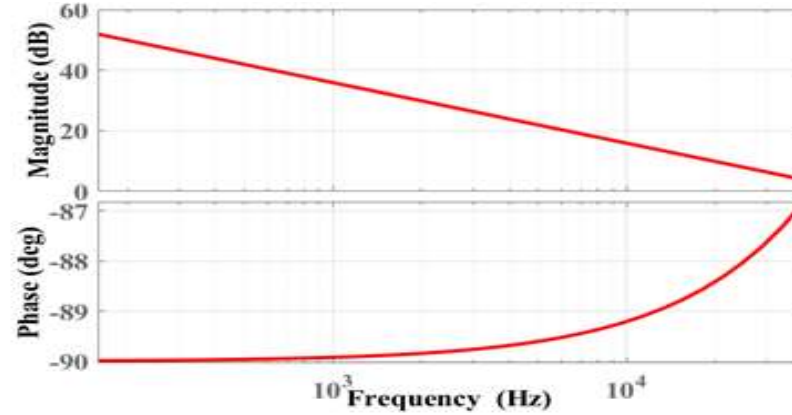
Time scale: 50us/div
(a)



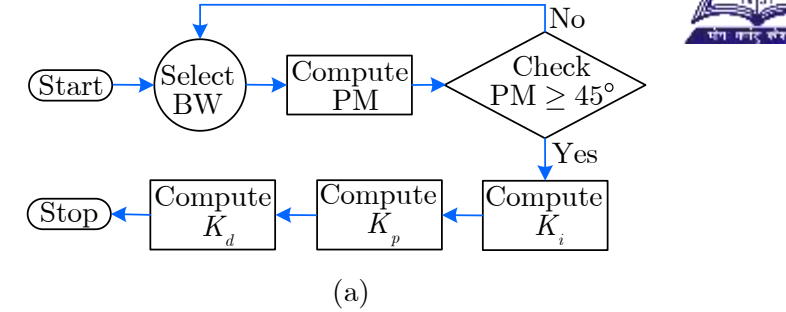
(b)



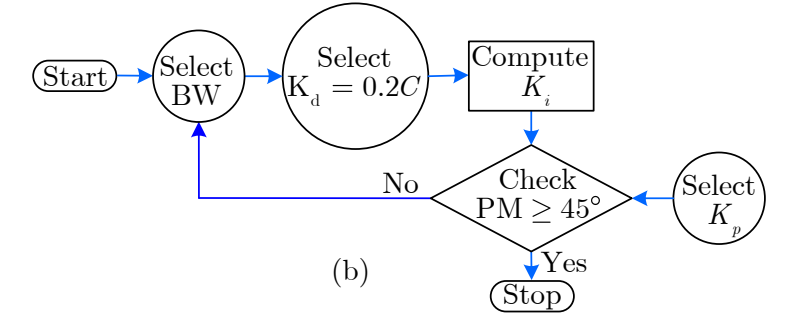
(c)



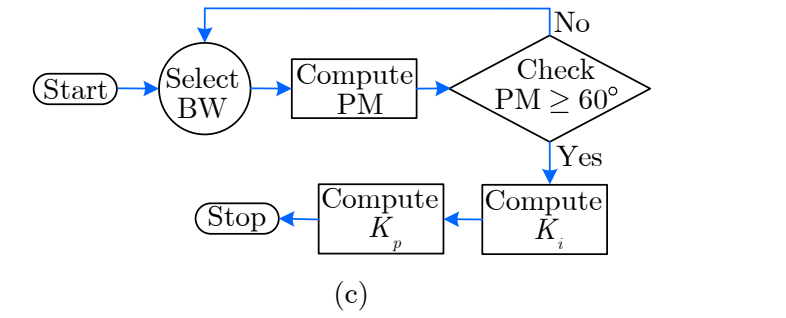
(d)



(a)



(b)



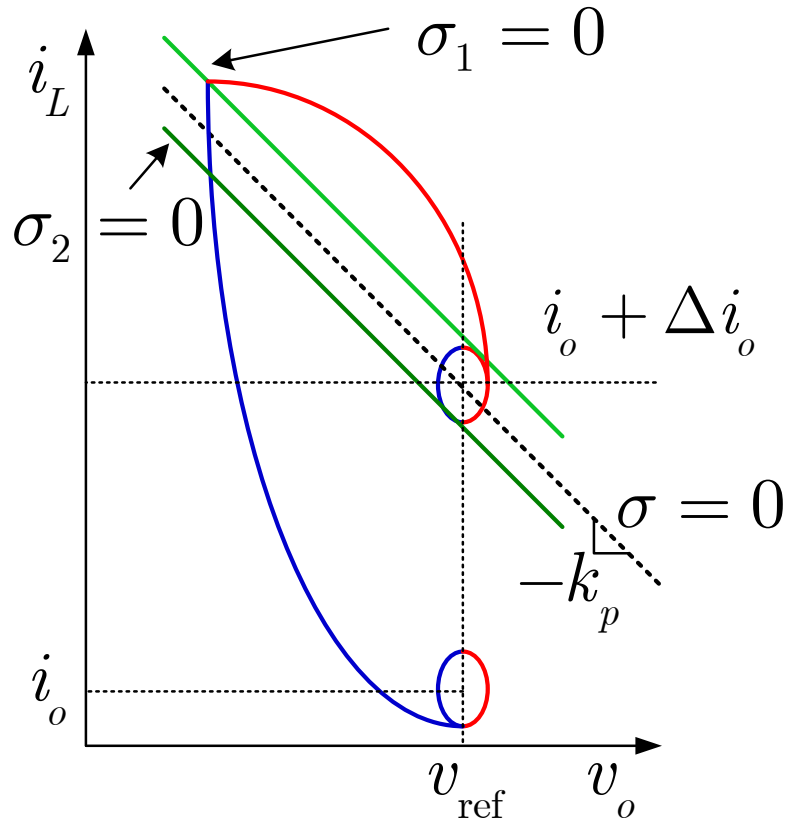
(c)

Load Transient of 10A using (a) DVMC (b) MCMC, Bode plot of (c) O/P impedance shaping under DVMC, (d) loop transfer function under MCMC

Flow chart of controller design (a) pole/zero cancellation, (b) alternative approach under DVMC, (c) pole/zero cancellation – MCMC

[A. Nanda, et. Al., "Frequency Domain Design Techniques in Digital Voltage ...", accepted, IEEE APEC 2023]

Large-Signal PID Controller Tuning in a VMC Buck Converter



$$\sigma = K_p v_e + \frac{dv_e}{dt} + K_i \int v_e dt = 0$$

- Proportional action – very fast and primary drives large-signal recovery
- Integral action – very slow compared to time optimal large-signal recovery

[Lecture~50, NPTEL “Control and Tuning Methods in Switched Mode Power Converters ...” on [YouTube](#)]



Large-Signal PI Controller Tuning Parameters for a Buck Converter

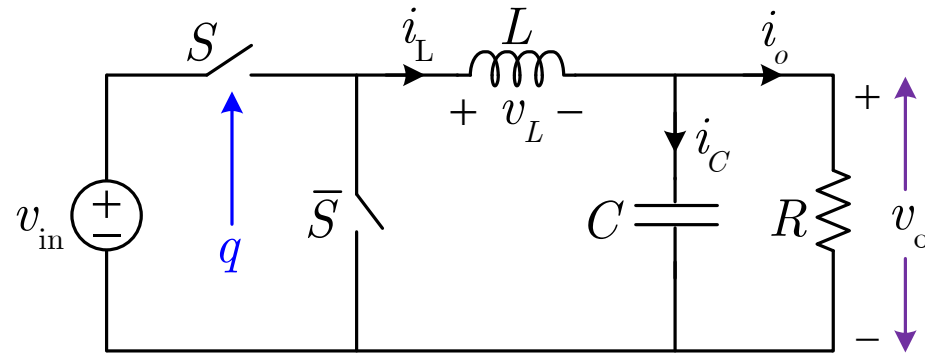
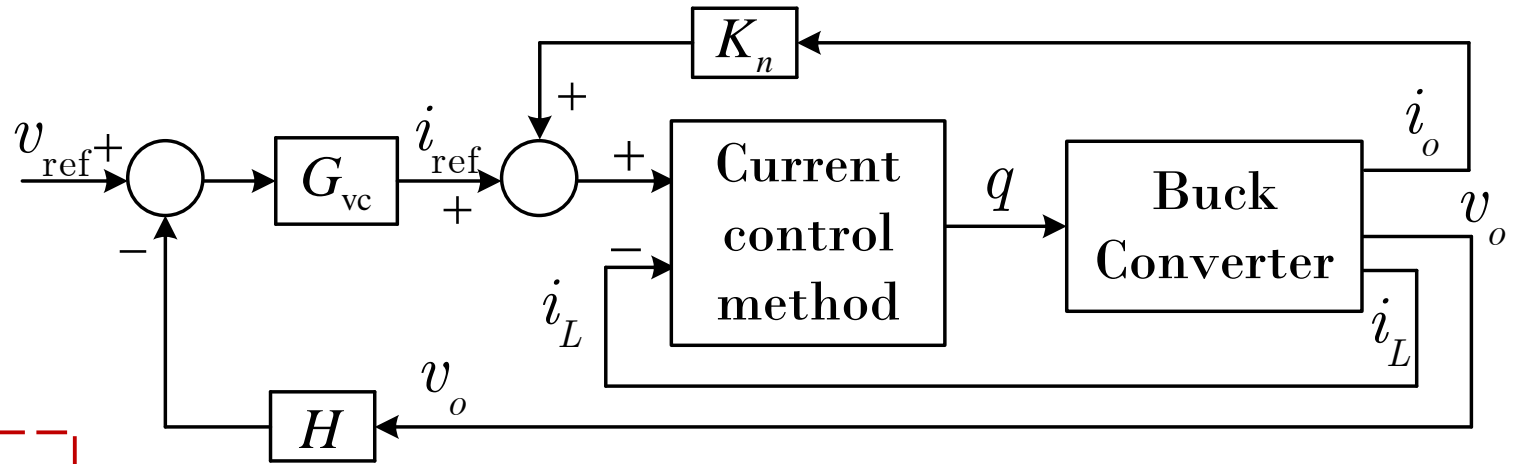
$$G_{vc} \ s = K_p + \frac{K_i}{s}$$

$$K_p \approx \frac{2C}{L\Delta i_o} \times \sqrt{v_{in} v_q}$$

$$v_q = \begin{cases} v_{ref} & \text{step-up} \\ v_{in} - v_{ref} & \text{step-down} \end{cases}$$

$$K_i = \frac{2\pi m_c + m_1}{10V_{in}}$$

$$k_n = 1$$



Lecture~48, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Large-Signal PI Controller Tuning Parameters – Practical Gains

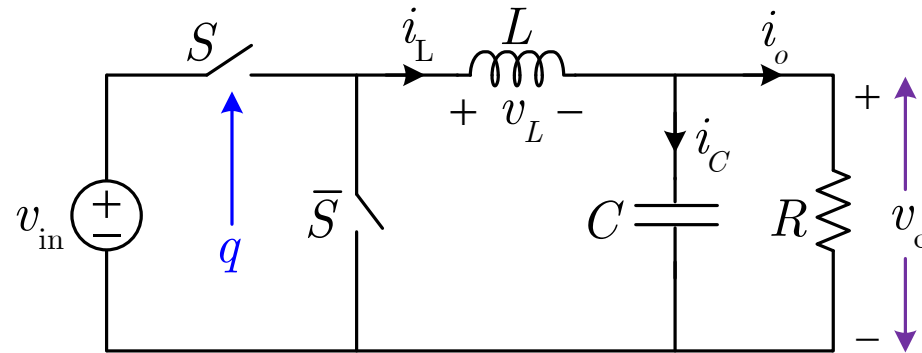
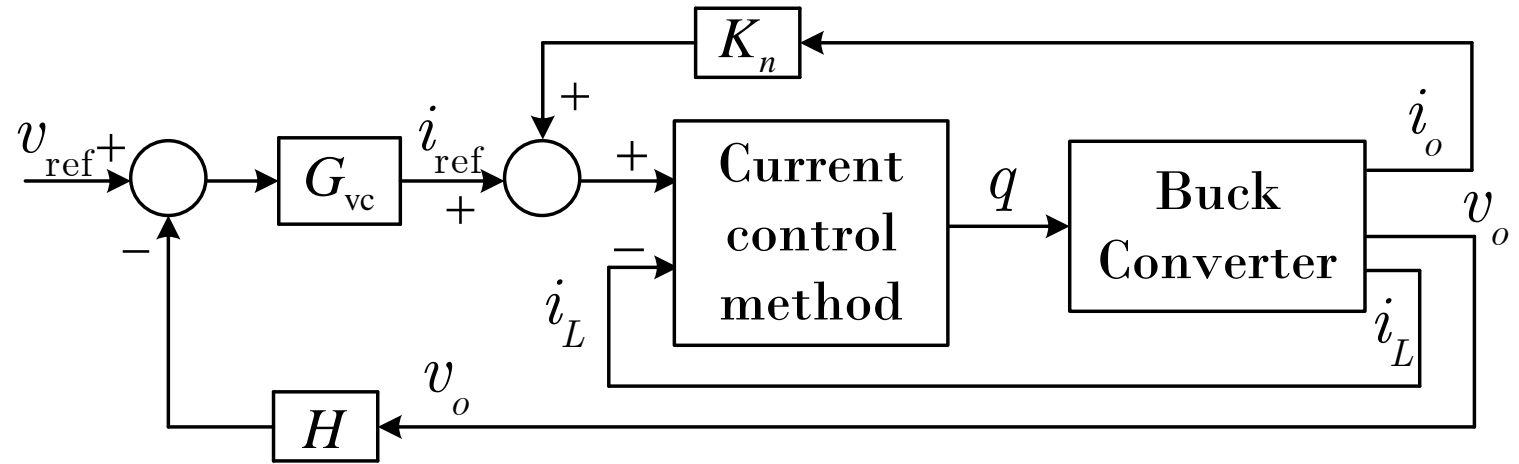
$$G_{vc} s = K_p + \frac{K_i}{s}$$

$$K_p \approx 20$$

$$K_{atten} \approx \frac{K_p}{K_{p,opt}}$$

$$K_i = K_{atten} \times \frac{2\pi m_c + m_1}{10V_{in}}$$

$$k_n = K_{atten}$$



Lecture~48, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Digital PI Controller in Mixed-Signal CMC Buck Converter

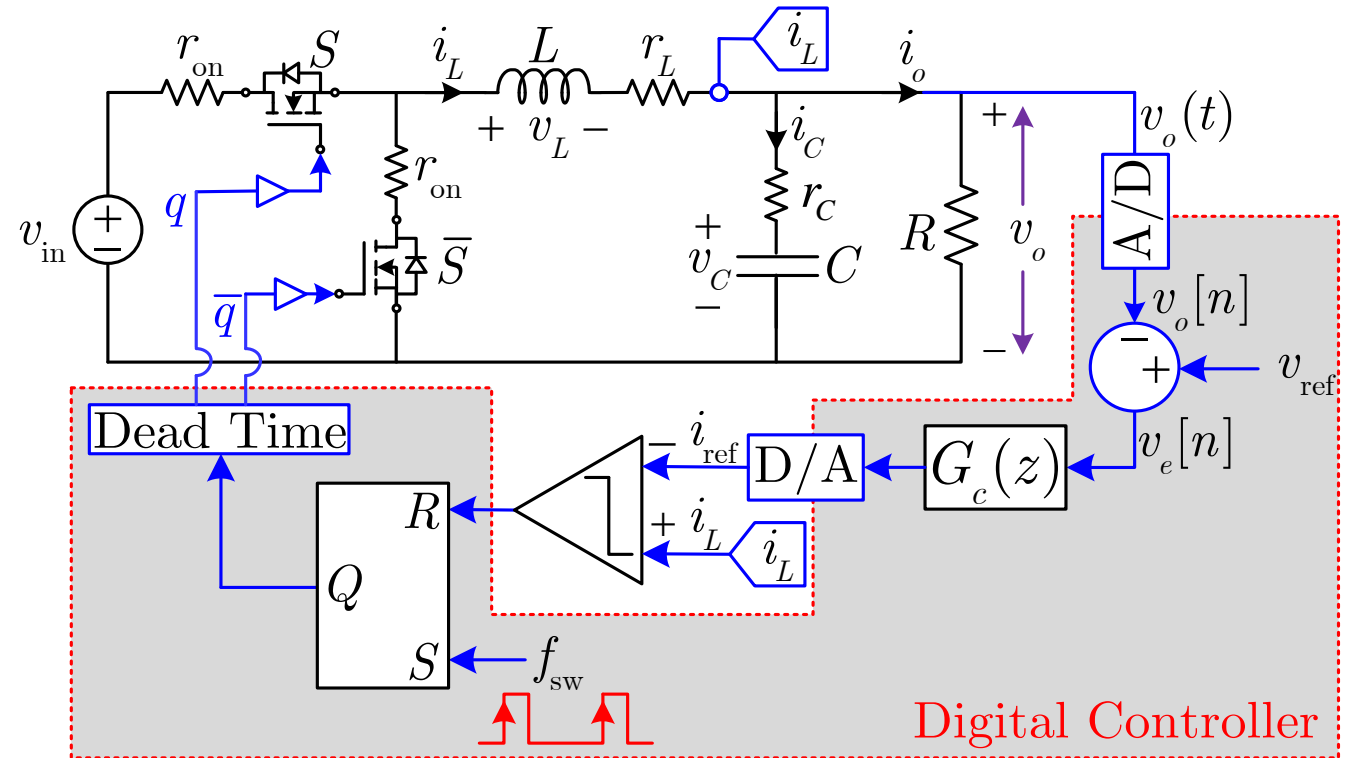
$$K_p \approx 20$$

$$k_n = K_{atten}$$

$$K_i = K_{atten} \times \frac{2\pi m_c + m_1}{10V_{in}}$$

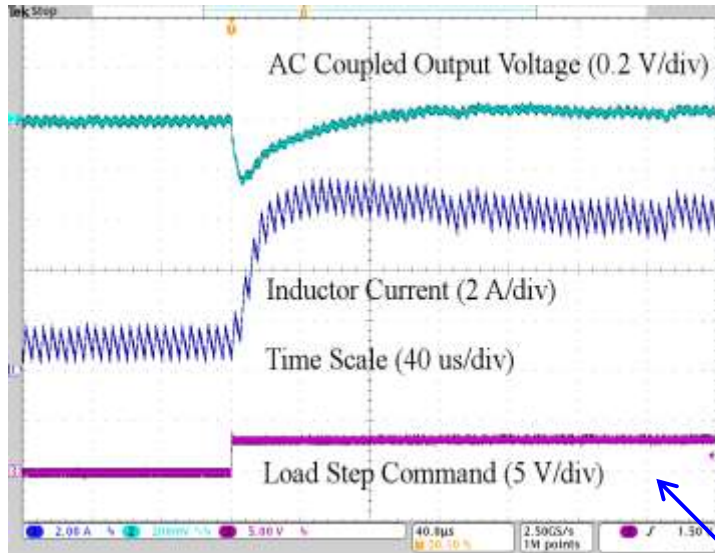
$$K_{pd} = K_p$$

$$K_{id} = K_i T_s$$



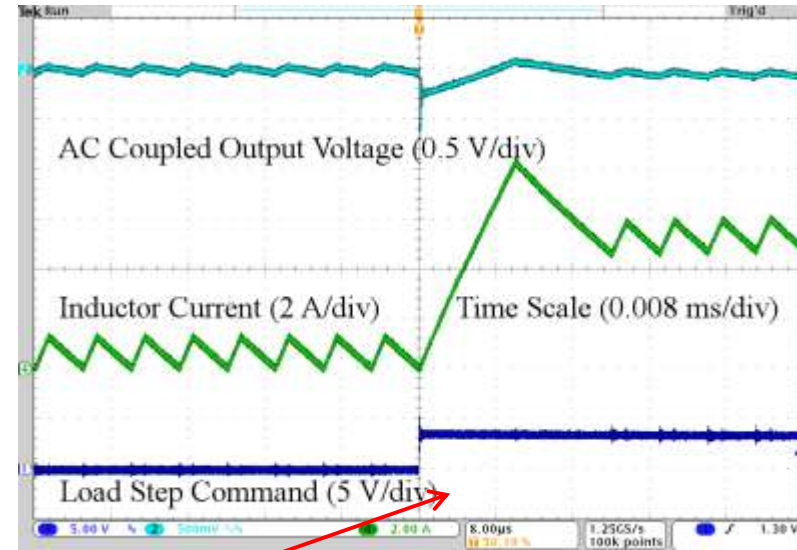
Lecture~43, Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)

Small-Signal vs. Large-Signal Tuning – Buck Converter



Relay-based PID tuning

I/p voltage: 9 V
 O/p voltage: 3.3 V
 Inductor – 10 uH
 Capacitor – 570 uF
 Freq. – 200 kHz
 Load current: 1-6 A



Parameter	Relay-based tuning	Large-signal tuning
Settling time (μ s)	96	16
Voltage undershoot (mV)	260	160
Current overshoot (A)	1.5	2.5
Eff. @ 1kHz load freq.	86.7%	90.6%

• **Step-up transient**

• **Optimal gain**

$$k_p \approx \frac{2C\sqrt{v_{in}v_{ref}}}{L\Delta i_o}$$

• **Only DPWM control**

I. Kumar & S. Kapat, “Unified Digital Current Mode Control Tuning ...”, *IEEE TPEL* 31(12) 2016

Small-Signal vs. Large-Signal Tuning Boost Converter

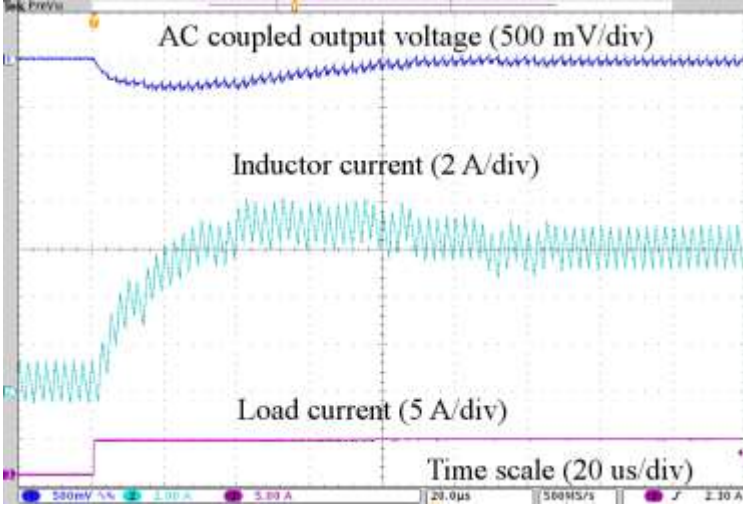
Specification:

$$v_{in} = 8 V, v_o = 12 V,$$

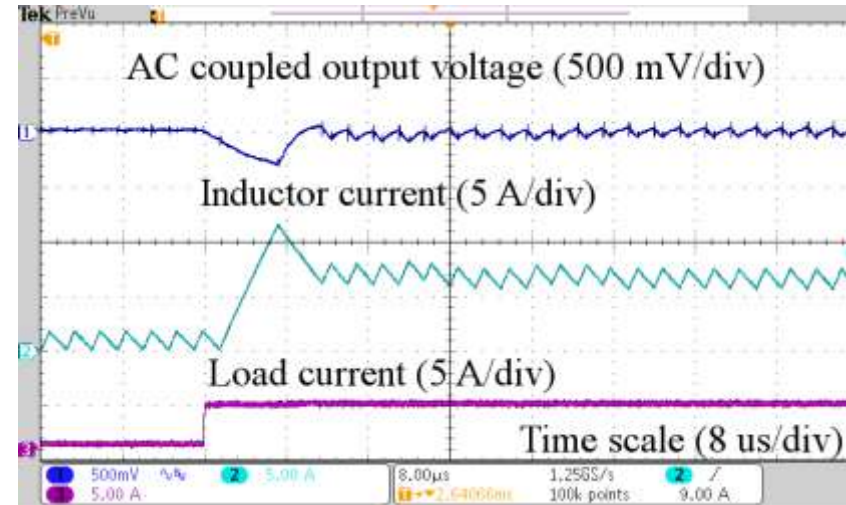
$$i_o \in [0.5, 5] A, L = 4 \mu H,$$

$$C = 100 \mu F, f_s = 400 kHz$$

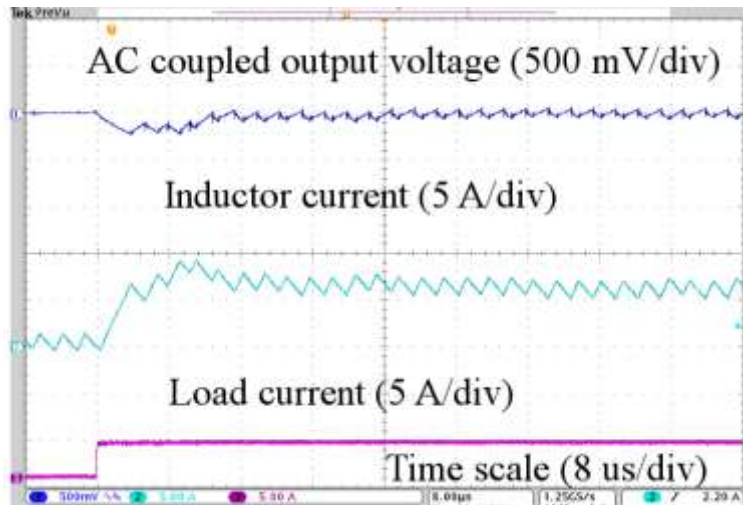
Parameter	Settling time	Peak undershoot
Linear Control	72 μs	320 mV
Large-signal (LS) tuning	8 μs	300 mV
LS tuning with v_o limit	11.2 μs	220 mV



Small-signal tuning



Large-signal tuning w/o limit

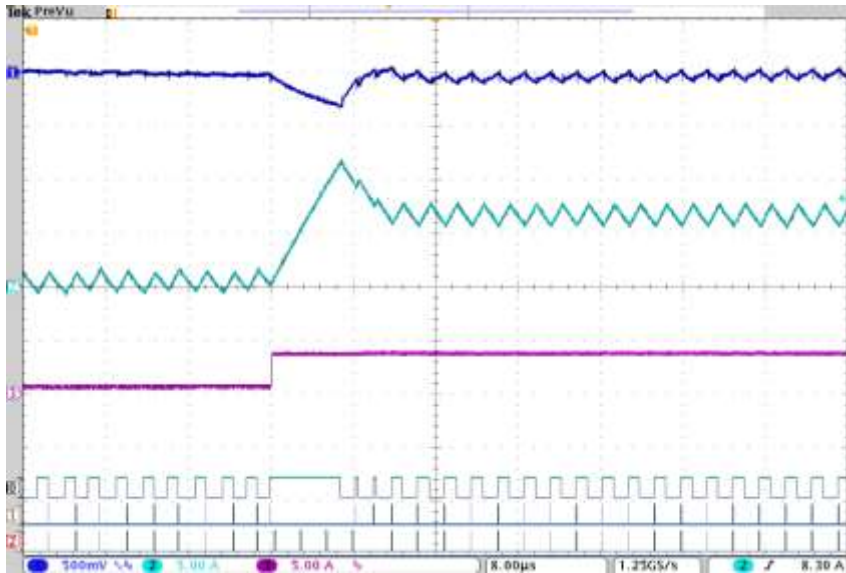


Large-signal tuning with limit

K. Hariharan, S. Kapat, "Near Optimal Controller Tuning in a Current-Mode ...", IEEE JESTPE, June 2019

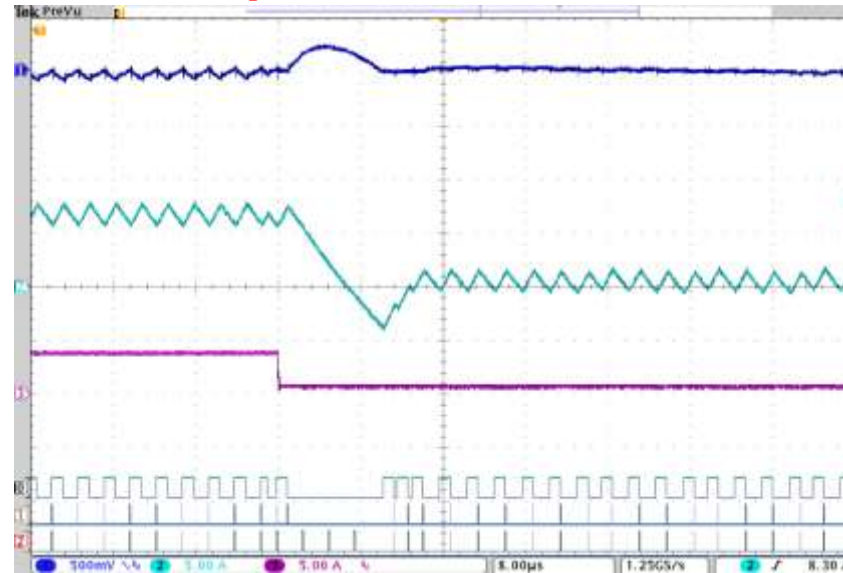
Large-signal PI Tuning in Constant On/Off-time Digital CMC Boost Converter

$$k_p = 16; k_i = 0.02$$



Step-up transient: Without time adaptation

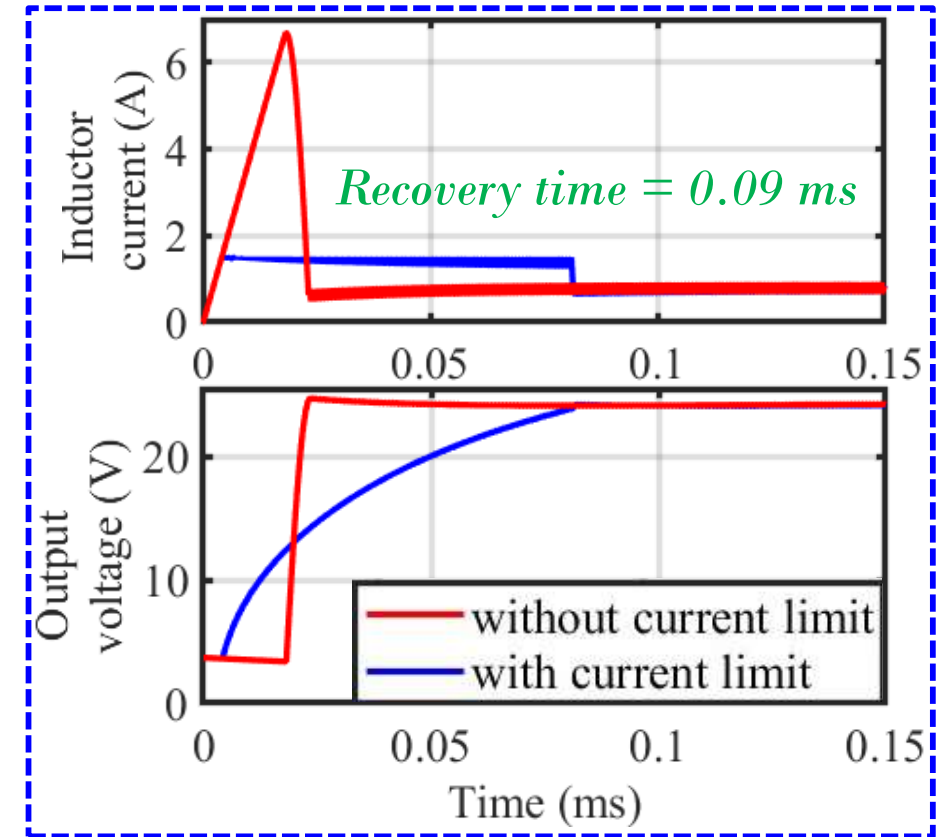
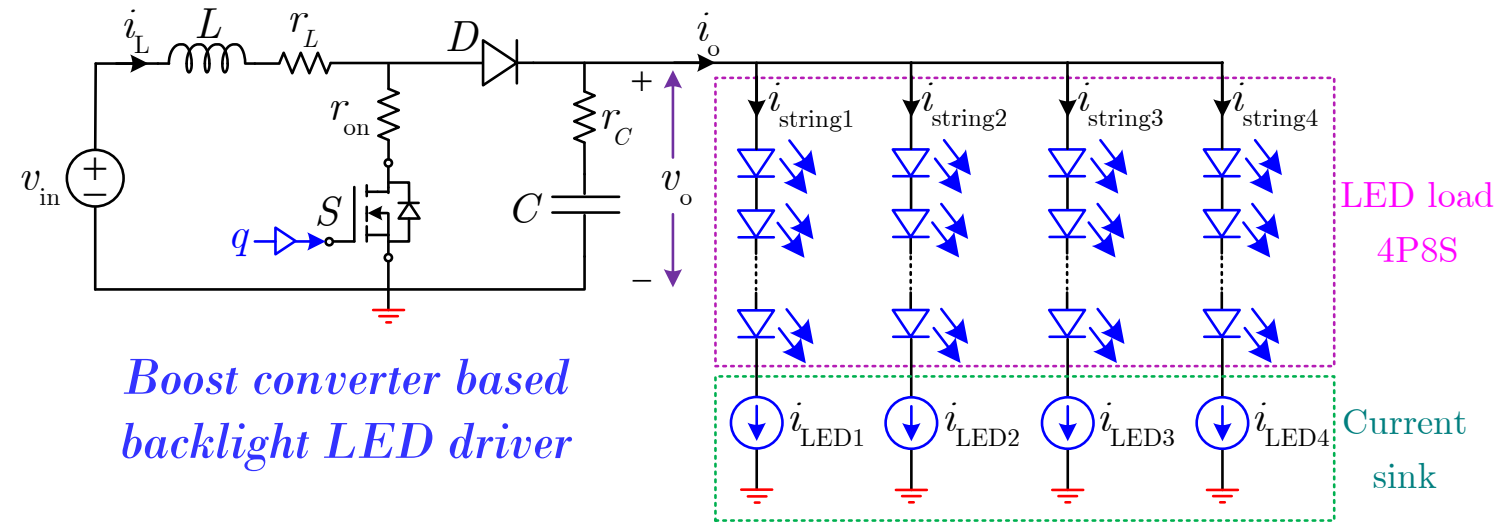
$$k_p = 32; k_i = 0.02$$



Step-down transient: Without time adaptation

[K. Hariharan & S. Kapat , "Online Controller Tuning in Current Mode Adaptive Off-Time ...," IEEE APEC, 2021]

Large-Signal Tuning – Constant Off-Time CMC Boost LED Driver



Start-up performance with FSC 30 mA/string

- ❑ Large-signal PI tuning in COFT boost LED driver
- ❑ Time-optimal start-up and dimming performance
- ❑ Under current limits, performance significantly improved compared to commercial LED drivers

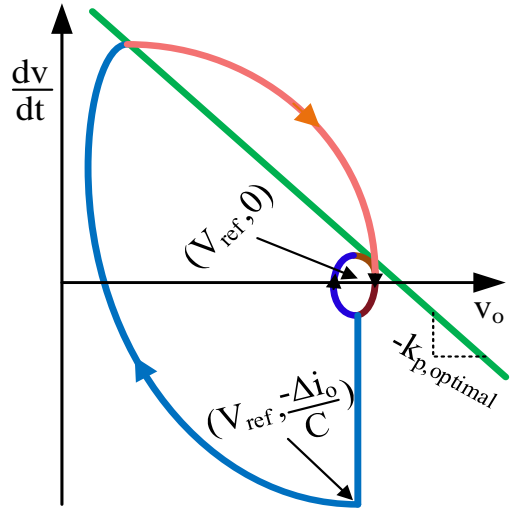
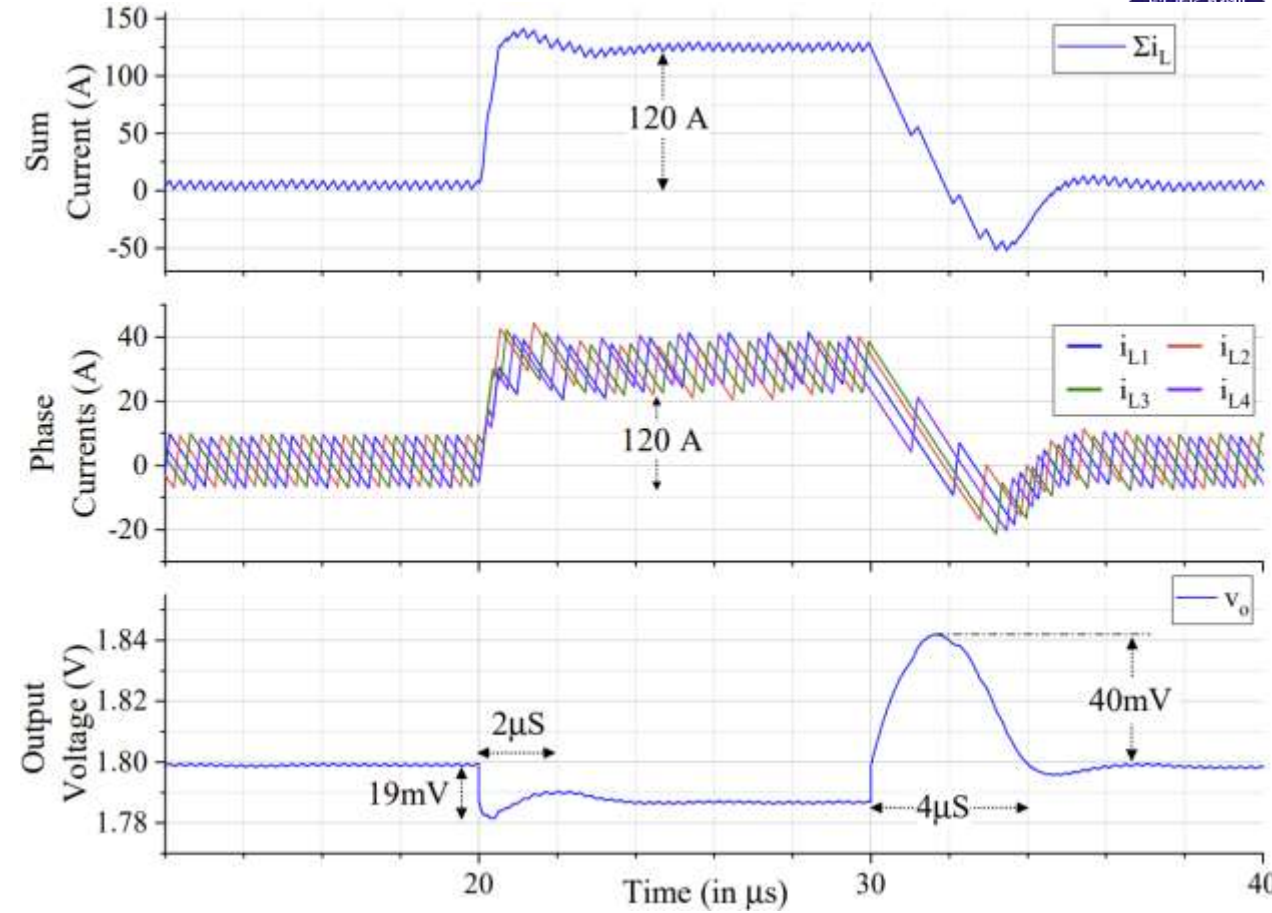
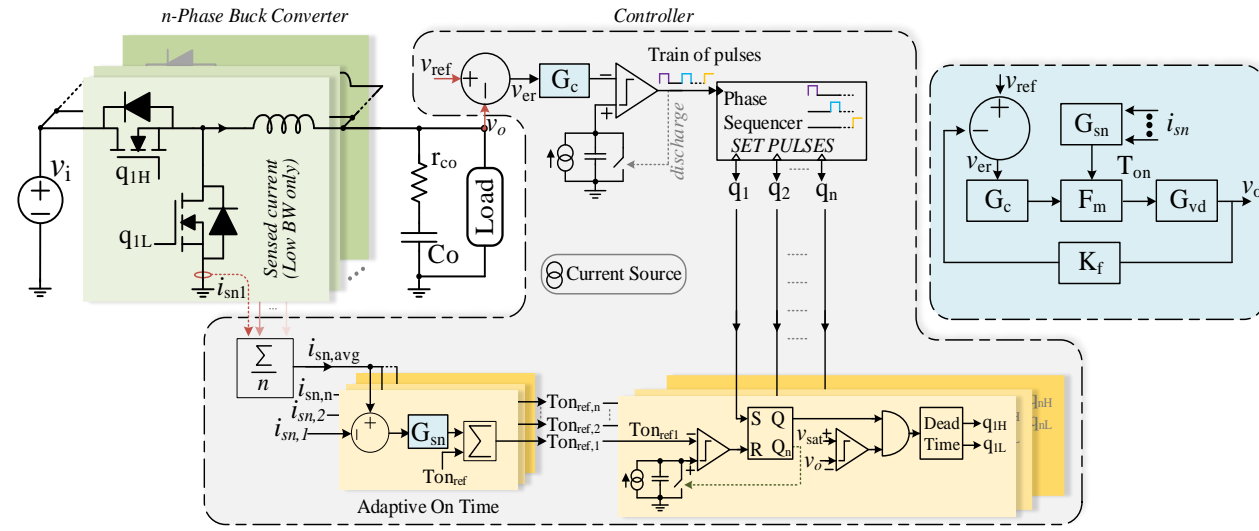
IIT Kharagpur and Qualcomm Collaborative Research Work

$$k_p = \frac{i_1 - i_{av}}{v_{ref} - v_{in}} \quad \text{where } i_1 = \sqrt{i_{av}^2 + \frac{1}{Z_c^2} (v_{ref} - v_{in})^2}$$

[D. Chatterjee, et. al., “Design Techniques in Constant On/Off-Time Peak Current ...”, accepted in APEC 2023]



Large-Signal PID Tuning – COT Multiphase Buck Converter

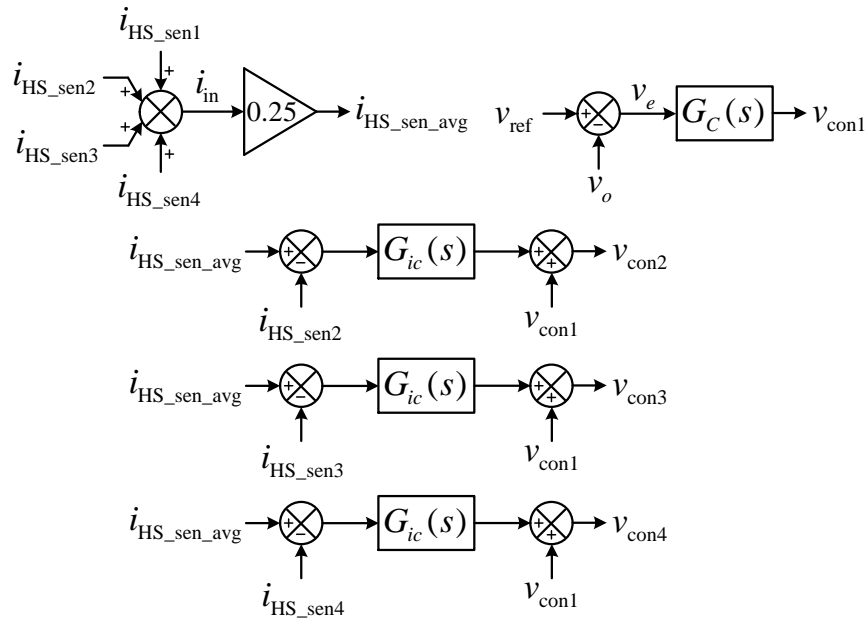


Sl. No.	Parameter	Value
1	V_{in}	12 V
2	V_o	1.8 V
3	L_{Phase}	100 nH
4	#Phase	4
5	$L_{effective}$	$\frac{L_{Phase}}{\#Phase}$
6	C_o	2 mF
7	ΔI_o	120 A

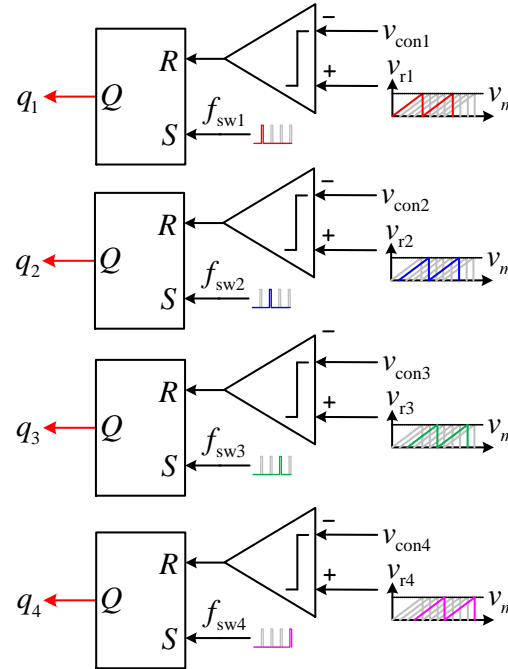
- ❑ Large-signal PID tuning rule developed
- ❑ Scalable approach for varying phase count

[P. Majumder, et.al., "PID Controller Tuning in Scalable Multiphase Buck Converters ...", IEEE ONCON 2022]

Large-Signal PID Tuning of VMC Multiphase Buck Converter



(a) High-side Low BW current sensing and compensation



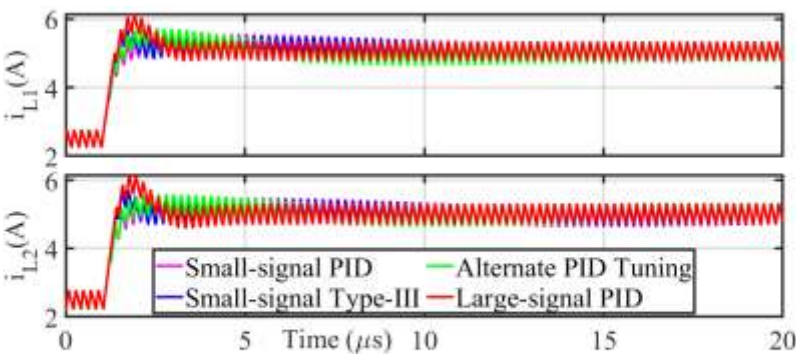
(b) Proposed VMC for equal current sharing

$$G_c(s) = K_p + \frac{K_i}{s} + \frac{K_d s}{1 + \tau_d s}$$

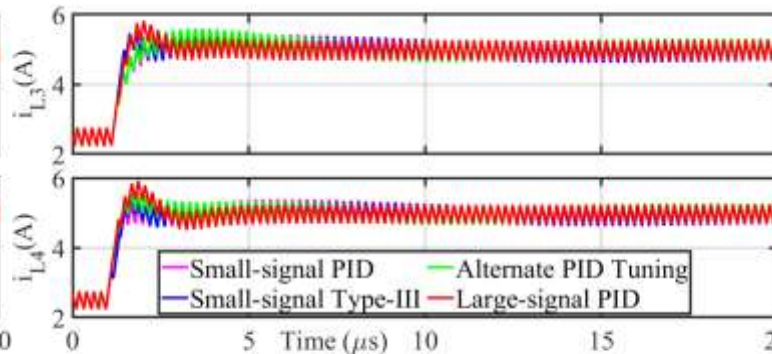
$$K_p = 20 \quad K_i = \frac{2\pi\Delta i_o}{C\sqrt{V_{in}V_{ref}}}$$

$$K_d = \frac{10L_{eq}\Delta i_o}{\sqrt{V_{in}V_{ref}}} \quad \tau_d = 10^{-7}$$

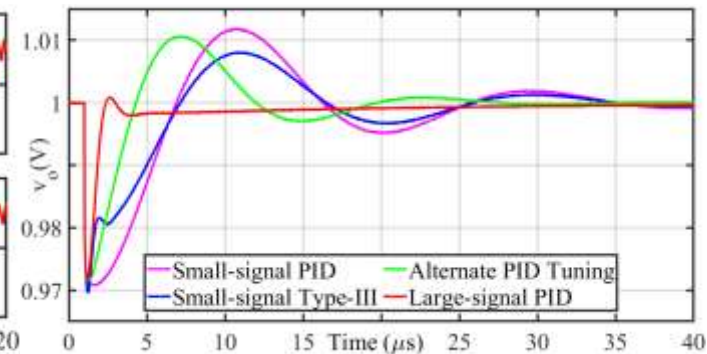
IIT Kharagpur and Qualcomm Collaborative Research Work



(a) Phase-1 and Phase-2 Inductor Currents



(b) Phase-3 and Phase-4 Inductor Currents

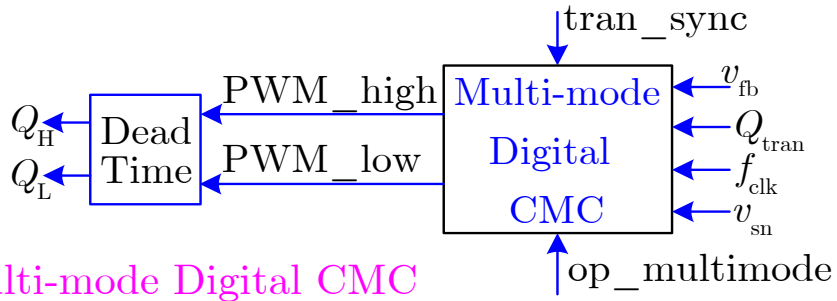
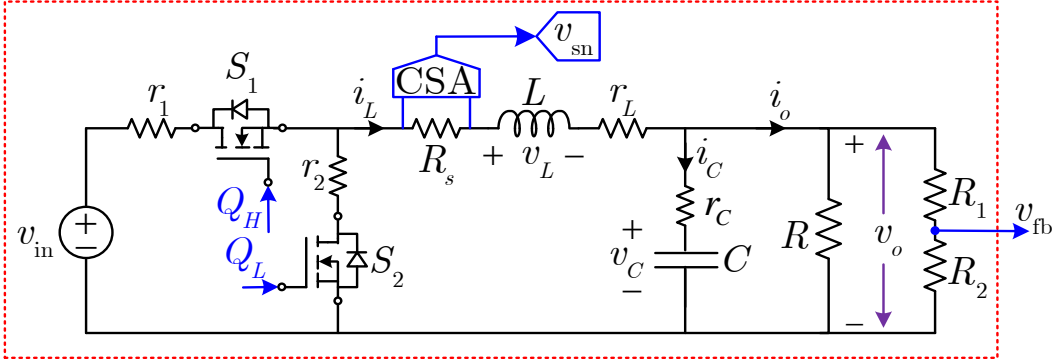


(c) Output Voltage

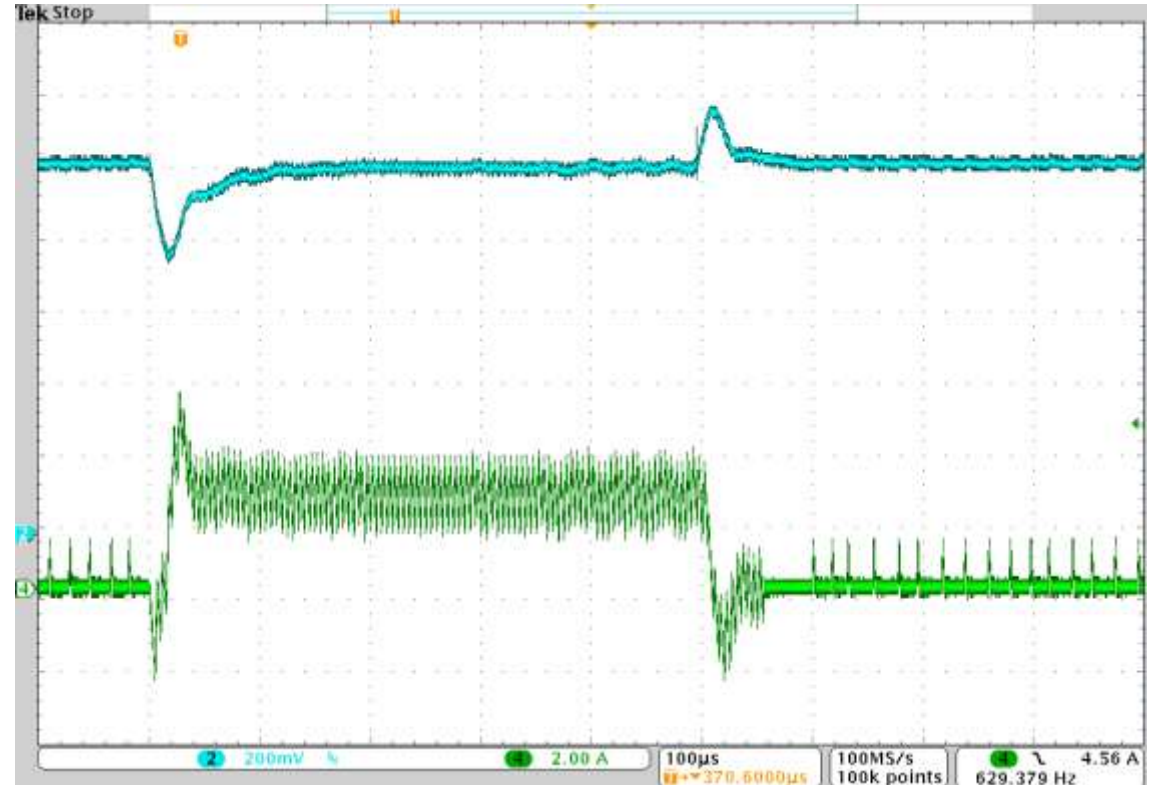
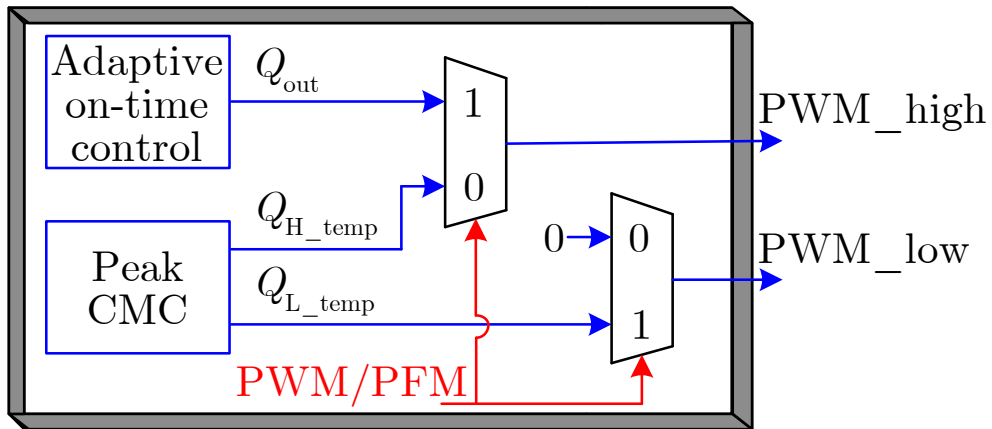
[T. Golla, et. Al., "Controller Design and Phase Current Balancing for Fast . . .," accepted in IEEE APEC 2023]

Peak Current-based PWM/PFM Multi-Mode Digital Control

Buck Converter



Multi-mode Digital CMC



Input Voltage V_{in}	3.3V
Reference Voltage V_{ref}	1V
Load resistance	13.5 – 0.322 Ω

K_p	4.64
K_i	0.4



Summary of Key Features using Digital Control in SMPC

- *Small-signal real-time tuning* – performance improvement using online tuning
- *Large-signal control and design* – ultra-fast load/reference transient response
- *Controller reconfigurations* – multi-mode digital control for fast transient & high efficiency
- *Dead-time optimization* – high efficiency & reduced EMI over a wide load current range
- *Scalability & portability* – scalable control and tuning, different process technologies
- *Hardware/software interface* – platform-independent control scheme, third-party interface

Digital Control Skillset Development – Pedagogical Perspectives



- Understanding digital control architectures (modulation, sampling, feedback/feedforward control law), modeling, analysis, small-signal and large-signal based design and tuning
- Understanding implementation platforms and programming language – such as FPGA (Verilog HDL), STM32, C2000 series microcontroller platforms (software, firmware , etc.)
- Introduced a new NPTEL Online Certification Course on “*Digital Control in Switched Mode Power Converters and FPGA-based Prototyping*” – [Available on YouTube](#)



Why is this Course?

- To familiarize digital control architectures with resource constraints, analysis/design tools*
- To introduce Verilog HDL coding, fixed-point implementation and FPGA prototyping*
- To demonstrate power converter hardware prototypes using Xilinx FPGA along with STM32 (from ST Microelectronics) and C2000 (from TI) microcontrollers*
- To present MATLAB customized model development & design validation*
- To develop skilled manpower and to enable indigenous IP development*

Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)



Summary of this Digital Control Course

W_1

Introduction to Digital Control in SMPCs

Fixed and Variable Frequency Digital Control Architectures

W_2

W_3

MATLAB Custom Model Development under Digital Control

Modeling Techniques and Model Validation using MATLAB

W_4

Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)



Summary of this Digital Control Course

W₅ Frequency and Time Domain Digital Control Design Approaches

Digital Control Implementation and FPGA based Prototyping

W₆

W₇ Introduction to Verilog and Simulation Using Xilinx Webpack

Digital Controller Implementation using Fixed Point Arithmetic
and Verilog HDL

W₈

Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)



Summary of this Digital Control Course

W_9

Digital Control Implementation using STM32 and C2000 series Microcontrollers – Software/Firmware Aspects with Hardware Demo

Steps for FPGA Prototyping of Digital Voltage Mode and Current Mode Control with Hardware Case Studies

W_{10}

W_{11}

Design and Validation Case Studies using Digital Voltage and Current Mode Control

Hardware Case Studies of Advanced Digital Control Techniques and Course Summary

W_{12}

Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)



Summary of Course Outcomes

- ❑ *Level of digitization in closed-loop switch mode power converters*
- ❑ *Modulation and sampling methods in fixed-frequency digital control*
- ❑ *Modulation and sampling methods in variable frequency digital control*
- ❑ *Custom model development using MATLAB Simulink for various architectures*
- ❑ *Overview of modeling techniques with their complexity and accuracy*
- ❑ *Modeling of closed-loop digital control and steps for model validation*

Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)



Summary of Course Outcomes

- ❑ *Design of fixed frequency digital voltage mode and current mode control*
- ❑ *Concept of Q format for fixed-point digital implementation using Verilog HDL*
- ❑ *Synthesizable Verilog HDL codes for fixed and variable frequency digital controllers*
- ❑ *Steps for Verilog HDL-based digital control implementation and FPGA prototyping*
- ❑ *Hardware prototyping and live demo with multiple experimental case studies*
- ❑ *Software/firmware for FPGA, STM32 and C2000 microcontrollers*
- ❑ *Verilog HDL synthesis for multimode digital control techniques*

Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)



Usefulness of the Course and Key Takeaways

- ❑ **Understanding digital control architectures, modulation and sampling techniques**
- ❑ **Selection of suitable digital control architectures based on application/cost requirements**
- ❑ **MATLAB custom model development for fixed and variable frequency digital control**
- ❑ **Modeling, analysis and design methods for fixed frequency digital control**
- ❑ **Verilog HDL programming – useful to synthesize digital architectures**
- ❑ **FPGA prototyping – useful for developing IP and validating design**
- ❑ **Skill manpower development – corporate R&D, product development**

Online course on “Digital Control in Switched Mode Power Converters & FPGA-based ...” on [YouTube](#)



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Akshat Jain



Aravindhan K.

Texas Instruments



Aditya Dholakia



Nitin Nigam

Keysight Tech.



Thank you